Analog – Voltage-to-Frequency Converter (Continuous Type)

AN58469

Author: Archana Yarlagadda
Associated Project: Yes
Associated Part Families: CY8C29x66, CY8C28xxx, CY8C27x43, CY8C24x94 CY8C24x23A, CY8C24x33, CY8C23x33, CY8C21x34, CY8C21x23
Software Version: PSoC Designer™ 5.0
Associated Application Notes: AN2161, AN2115

Application Note Abstract

This application note describes a PSoC® 1 based wide range, continuous-time Voltage to Frequency (V-to-F) converter. The converter is based on high frequency relaxation oscillator circuit. This type of converter is used in applications such as FSK modulators, voltage or current regulators, and ADCs.

Introduction

This application note describes a V-to-F convertor with continuous time block. The implementation is in hardware and the CPU is not used during the operation. The goal is to implement a wide range, continuous type voltage-to-frequency converter. Another type of a voltage to frequency converter is described in application note AN2161 *'Voltage-to-Frequency Converter'*. It uses two analog PSoC blocks: a switched capacitor (SC) block as an integrator, and a continuous time (CT) block as a Schmitt trigger. This structure has a disadvantage because of the sampling nature of its operation. It limits the types of applications for the following reasons:

- Low operation frequency (up to 10 kHz)
- A jitter in the output signal not suitable for audio applications

The method described in this application note uses two passive external components: a resistor and a small integrating capacitor. The advantage of this method is the high frequency operation. However, the disadvantage is that the response is not linear, as explained in a later section. Along with the square wave output, a triangular waveform can also be obtained with this circuit. For other methods of generation of waveforms, refer to AN2115 *"Generate Triangle and Trapezoid Waveforms with a Switched- Capacitor Integrator".*

V-to-F with Relaxation Oscillator

The circuit discussed in this application note is built using one programmable comparator (CmpPrg) as shown in Figure 1. The digital buffer (DigBuf) is used to provide flexibility to route to any pin on the package. To save a digital block, the signal from the comparator can be directly connected to the global bus by writing the register CMP_GO_EN. Complete details about this register is available in the Technical Reference Manual (TRM).

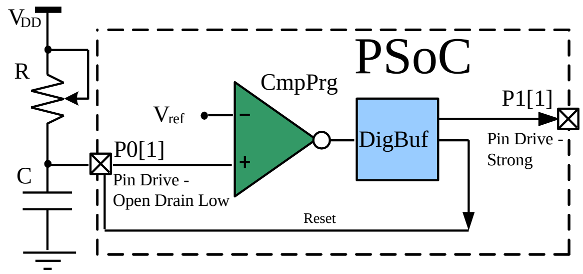
The comparator bus, which is used to pass the signal from the CmpPrg to the DigBuf user module, has its own latch that samples the signal. To avoid interference between the column clock and the generated signal, the comparator bus must be unsynchronized and the latches must be transparent (output tracks the input). CMP_CR1 register is used to bypass the synchronizing of the comparator bus with column clock, and ACBxxCR2 register is used to make the comparator latch transparent. The following code illustrates the settings required. For more information on these registers, refer to the TRM.

```
CMP_CR1 |= 0x10;
//Unsynchronize comp bus & column clk
CMPPRG_1_COMP_CR2 &= ~0x40;
// ACBxxCR2 CLatch is set transparent
```

Note that the digital signal from the CmpPrg must be inverted. In the project accompanying this application note, this is done by the 'NOT' function of the LUT of the comparator bus. Other possible ways are by using 'InvertInput1' parameter of the DigBuf User Module or the 'NOT' function of the digital row LUT.

[+] Feedback

Figure 1. Relaxation Oscillator



Circuit Operation

The schematic of the circuit is provided in Figure 1 and the operation waveforms are provided in Figure 2. Initially, the capacitor C is discharged and the pin P0[1] is at '1'. The open-drain low drive acts as 'High-Z' for an output of '1' and 'Strong' for an output of '0'. The capacitor C is exponentially charged (see Figure 2) through resistor R. When the voltage on capacitor C reaches the threshold level V_{ref}, the comparator (CmpPrg) trips and the capacitor C is discharged through pin P0[1]. At the same time, the CmpPrg is triggered into the initial state. A periodic process is possible because of a propagation delay t_d (about 0.1 µs) from the input of CmpPrg to the output driver. This delay allows the discharge of capacitor C before the output driver is returned to the initial state. The main operation condition is that the discharging time must be less than the delay.

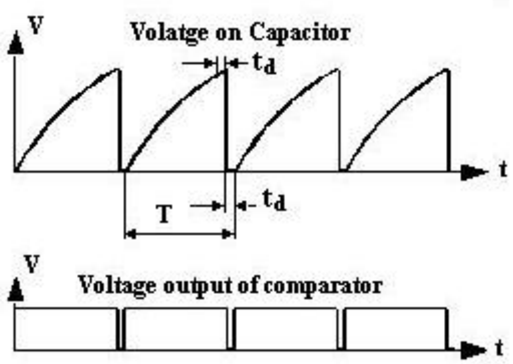
To find the period T, use Equation 1

$$T = RC \ln\left[\frac{V_{DD}}{(V_{DD} - V_{ref})}\right] + 2t_d \quad \text{Equation 1}$$

In the case $t_d << T$, the parameter t_d is ignored. If the external capacitor is comparable to the input capacitance of the pin, which is 10 pF, the sum of both capacitors must be considered. The output frequency is F = 1/T.

In Figure 1, the relaxation oscillator is based on long charging and short discharging process.

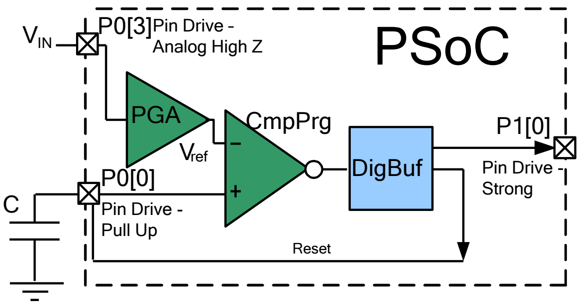
Figure 2. Operation Diagram



This structure has the disadvantage of including the potentiometer R into a signal loop. The schematic can be modified such that Vref is varied in place of R as shown in Figure 3.

The drive mode of the pin is set to "pull up". The nominal value of an internal pull up resistor is 5.6k. For more accuracy, use the external pull up resistor.

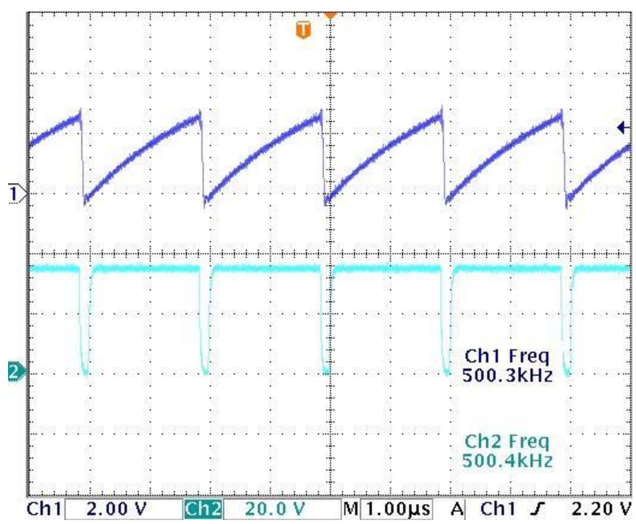
Figure 3. Relaxation Oscillator Controlled by Voltage (V-to-F Converter)



Test Results

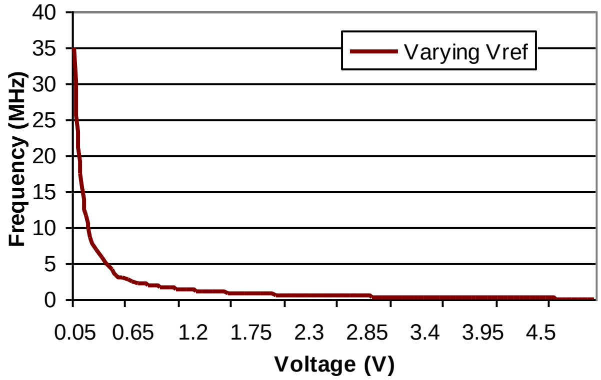
Figure 4 illustrates the test results for the schematic (shown in Figure 1). The values used are C = 470 pF, R= 5.2 kΩ, V_{DD} = 5 V, and Vref = 2.5 V (based on the settings in the CmpPrg). The expected frequency using equation 1 is 513 kHz; the frequency observed is 500 kHz.

Figure 4. Output Waveforms of Relaxation Oscillator



In this type of implementation, the variation of frequency is not linear with voltage, as shown in Figure 5.

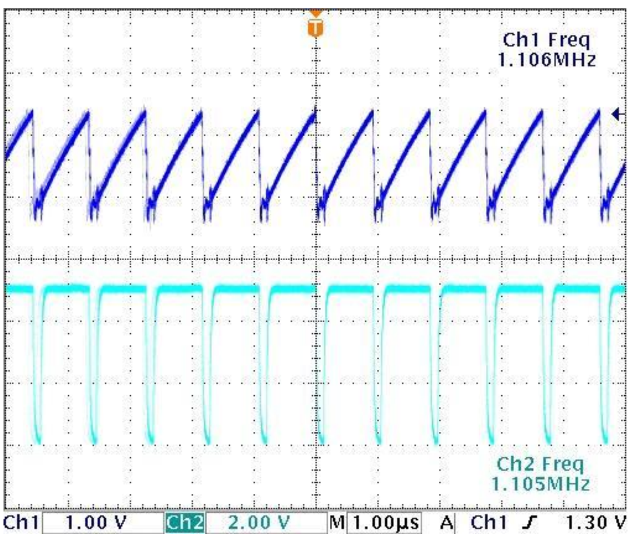
Figure 5. Frequency Variation with R and Vref



The graph is plotted with the assumption that the internal resistance is 5.6 kΩ. The Vref is calculated by resistive divider method from Vdd.

Consider the input of PGA as V_{in} = 1V. With the "LowLimit" of the comparator set to the output of PGA and its "RefValue" set to 0.021, Vref = 1.1V. The expected frequency for this setup, using equation 1 is 1.5 MHz. The measured value is 1.1 MHz, as shown in Figure 6.

Figure 6. Output Waveform of the V-to-F Convertor



The deviation in the expected from observed is because of the approximation of the pull-up resistor and the external capacitor. The capacitors are typically not precise and vary with temperature and voltage. So, the V-F relationship varies based on the variation in capacitance.

In applications which require precise frequency for a given voltage level, a single point calibration can be achieved with voltage output Multiplying Digital to Analog convertor (MDAC). The MDAC output can be used to tune the frequency, using internal main oscillator's reference and V_{ref} as an input. By setting the voltage using the MDAC, the V-to-F relationship is more predictable.

Summary

There are different types of V to F converter implementations and this application note shows one such method with PSoC. The advantage of this method is its high frequency operation; the non-linear response is a disadvantage.

Acknowledgment

This application note is based on the material presented in "V-to-F Converter (Continuous Type) and Wind Noise Simulator - AN43171 " by Ilya Mamontov, which is no longer available on the Cypress website.

[+] Feedback

About the Author

Name:	Archana Yarlagadda
Title:	Applications Engineer
Background:	Archana works as an Applications Engineer in Cypress, with a focus on PSoC. She has a Masters in Analog VLSI from University of Tennessee, Knoxville
Contact:	yara@cypress.com

Document History

Document Title: Analog – Voltage-to-Frequency Converter (Continuous Type)

Document Number: 001-58469

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2829378	YARA	01/06/10	New application note

PSoC is a registered trademark and PSoC Designer is a trademark of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein may be the property of their respective owners.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com/

© Cypress Semiconductor Corporation, 2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

This Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.