Reducing guesswork in ESD tests

Transmission line pulse measurements on the front end of the compliance phase can minimise the guesswork.

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Passing an ESD compliance test often makes an engineer's day. Your product has jumped one hurdle on the way to market. Management is pleased, and you leave feeling that you've done your job well. But ESD problems can lurk under the surface. You need to understand why a design passes or fails.

One shortcoming of system-level ESD compliance is the test's binary pass/fail nature. In ESD compliance testing, a product's vulnerable stress points and data ports are zapped with ESD strikes per the desired immunity standard. The product passes or fails. A "fail" condition means a data port IC had physical damage that disrupted the system's operation, or the system experienced a software upset/reset during the testing. A "pass" condition typically means there was no observable physical damage or soft reset, and the equipment can still maintain a link, recover, or operate in a certain specified state after the ESD strikes.

Regardless the test result, there are many unknowns. If the product passed ESD compliance, by how much safety margin did it pass? If this margin is thin, is there a danger of latent failure? Could small, incremental ESD damages aggregate to weaken an IC and eventually result in full device failure?

There are even more questions if the product failed ESD compliance. What stress points and/or interfaces failed? Can the failure threshold be quantified? How much protection and/or PCB routing changes are needed to harden the interface and bring the product into compliance? You simply don't know in a pass/fail test.

With the compliance phase as a barrier to time to market, engineers with passing documentation in hand are eager to leave the compliance lab and hand the product to marketing. Yet a short-term outlook is of little value when ESD problems arise again on future designs. System designers and EMC engineers need a more methodical approach to quantify some of the unknowns. Transmission line pulse (TLP) testing is one method that can help quantify ESD failure thresholds.

TLP measurements have long been used in the electronics industry to characterise the ESD immunity and robustness of on-chip/internal protection structures. In recent years, the TLP technique has also been applied to system-level transient protection devices. Today it is quite common for protection device manufacturers to put TLP data in their datasheets to highlight the performance of their system-level ESD clamps. In this context, the TLP test uses high-current, short-duration pulses to generate IV (current vs. voltage) data that characterizes the semiconductor device under test (DUT).

A typical TLP setup consists of a TLP generator that injects discrete 100 ns square-wave current pulses into a DUT. The 100 ns value nicely approximates the duration and stress of the ESD event. For a single TLP square pulse, the output pulse current is measured, and then the reflected voltage from the DUT is measured. The pulse current is stepped up in a determined increment and the measurement is repeated. Successive measurements create the IV curve data.

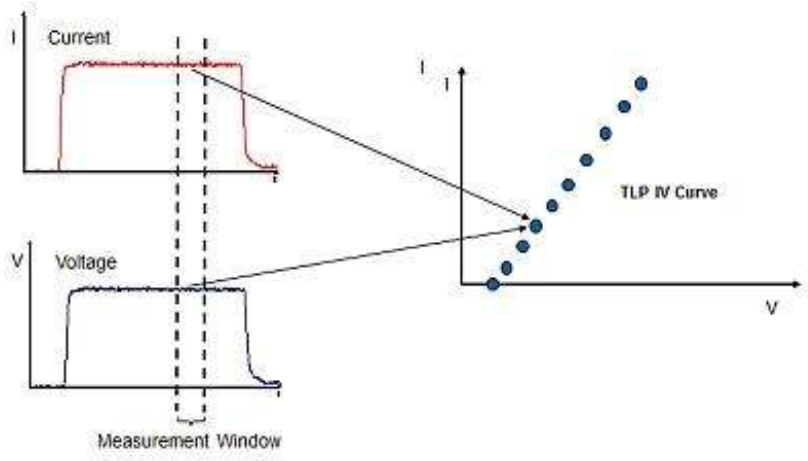

Figure 1: A transmission line pulse (TLP) IV curve plots current versus voltage.

Measure dynamic resistance

The IV curve of a protection device shows some interesting things about the clamp structure's behaviour. You can see at what voltage the device will begin to exhibit low impedance (i.e., turn-on or trigger voltage). You can also see the protection clamp's damage threshold, which is generally observed as a sharp secondary snapback in the IV curve. This snapback hints at when the protection element begins to sustain damage. Most TLP generators also allow for monitoring the DUT's leakage current.

When you examine the leakage current data of the protection device alongside the IV curve, you can isolate and confirm the current pulse at which the ESD protection element would be damaged by an ESD pulse (I_F or the failure current). The other important metric that the TLP data gives us is the ability to measure the dynamic resistance (R_{DYN}). This is typically defined as the slope of the IV curve, generally from 4 A to 16 A (as shown below). Protection device manufacturers use TLP data to characterise the dynamic resistance (R_{DYN}) of their ESD clamps. You can think of R_{DYN} as a measure of how well the transient voltage suppression (TVS) device is clamping -- ignoring the turn-on voltage, of course.

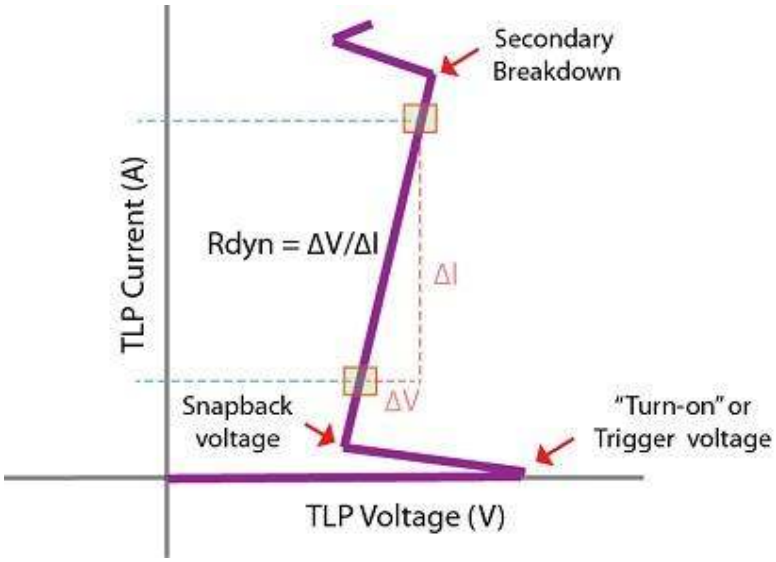

Figure 2: A TLP IV curve shows turn-on voltage, dynamic resistance (R_{DYN}), and secondary breakdown.

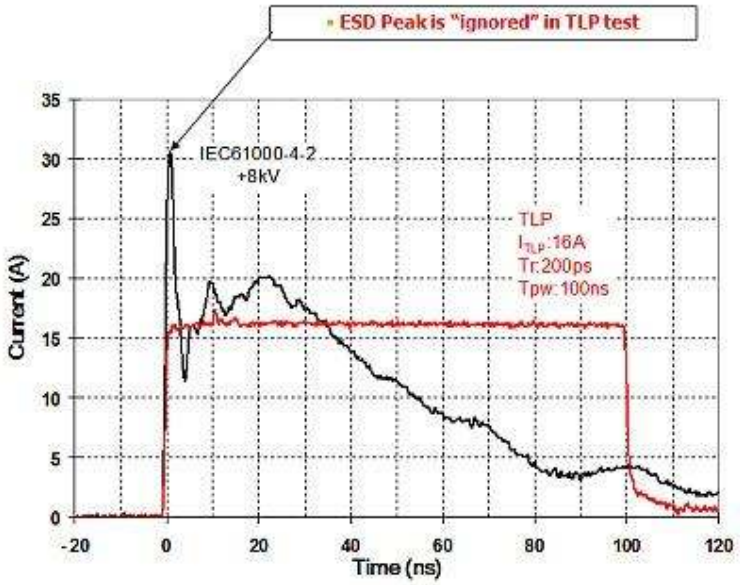

Figure 3: A +8kV IEC61000-4-2 waveform comparison to 16 A, 100 ns TLP waveform shows how TLP pulse lacks the initial peak.

One advantage of the TLP measurement technique is that the square pulse removes much of the variability in the system-level ESD test. Figure 3 shows the waveform of a +8 kV ESD pulse per the IEC61000-4-2 (black curve) plotted alongside a 16 A TLP pulse (red curve). You can think of the system-level waveform as the superposition of two waveforms: the initial first spike (a metal-to-metal interaction) and the discharge from the body resistance of a

human body. This first peak varies greatly depending upon the inductance of the test setup/PCB. The TLP test essentially ignores the effects of this first peak. It approximates the energy due to the body resistance. For system-level protection, the first peak must be considered in the analysis. For now, however, we will ignore the first peak.

Predict off-chip protection

The TLP IV curves are exceedingly helpful in predicting the viability of an off-chip protection element to safeguard an IC interface. Here is a simple example. Suppose you have a high-speed data line driven by a 40 nm controller IC. If you generate a TLP IV curve of this interface (without external protection), you can determine the TLP current at which this device will begin to fail.

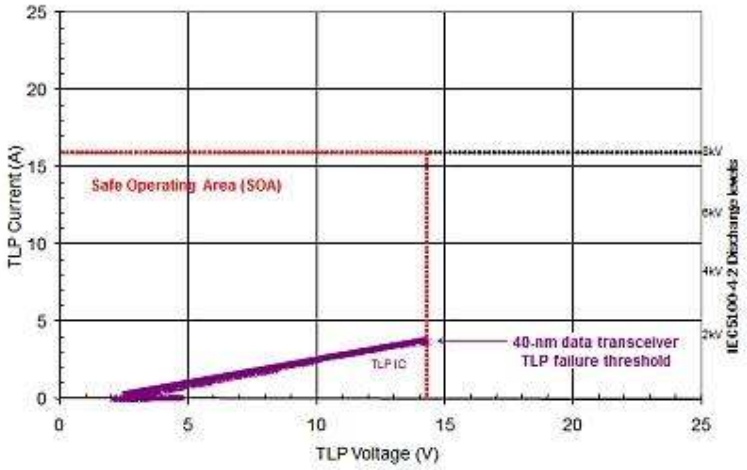

Figure 4: When the voltage reaches a threshold, a device fails.

You can then generate a TLP IV curve for a protection element alone on a separate test fixture. By overlaying these two curves and observing if the protection device's IV curve falls within the designated design window (8 kV by the IEC61000-4-2 standard), we can make a reasonable prediction of the viability of the protection component to safeguard the interface.

Figure 5 shows an example of TLP data of TVS protection devices (green and blue lines) superimposed upon the TLP curve of our 40 nm data transceiver (purple line). In this case, TVS A (in green) would pass the system-level ESD test to beyond 25 A (12.5 kV by the IEC61000-4-2). TVS B (in blue) would pass only to roughly 9 A (4.5 kV). We now have data that not only shows a protection device that should pass the system-level test, but also gives a more quantifiable picture of the protection margin that the TVS component offers.

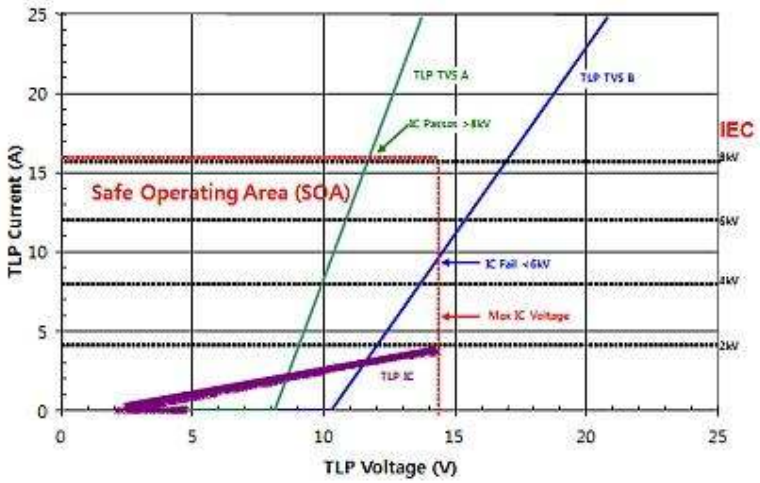

Figure 5: Protecting a high-speed data transceiver IC against ESD threats can improve immunity at compliance testing and in the field.

Before claiming victory, you must go back and look at the effects of the first peak of the ESD spike. Through the peak's duration, damage to sensitive oxide layers can and does occur. Even though the TLP analysis ignores the first peak, you can't ignore it in your ESD analysis. The best way to test the interface's vulnerability to the initial ESD spike is by applying the standard system-level discharges from the ESD generator. Assuming this testing does not

reveal latchup errors or any ESD-related damage, we can be reasonably confident that we have dialed in a good protection solution.
Since EMC engineers are often left with many unknowns during the ESD pass/fail compliance test, TLP measurements on the front end of the compliance phase can reduce some of the guesswork. The TLP analysis described above can be a very effective way to make good predictions on the effectiveness of an ESD protection device. TLP not only helps to quantify the level of ESD safety margin built into your protection scheme, but it also can save valuable time to market in the process. ■

About the author
Timothy Puls is Product Marketing Engineer at Semtech.