MOSFET selection for cellular phones

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Abstract

Travel time for business people has increased greatly, causing them to rely more and more on their cellular phones and notebook computers to conduct daily business transactions. With the usage time of these portable products being directly related to the life of the battery, designers are faced with the challenge of improving the power management of these products. Advances in discrete semiconductors and integrated circuit technology are allowing designers the ability to meet the challenge of extending battery life. This paper will focus on the cellular phone and discuss the various Power MOSFETs offered in the market for cellular phone application and the trend toward Application Specific MOSFETs. Elements in power management, power conversion will be discussed in relation to the selection of the most appropriate and cost effective MOSFET. Recent advances in power discrete wafer and packaging technology, significant device parameters and specifications and design examples of Power MOSFETs used in today's cellular phones, resulting in reduction in size and weight will be discussed.

Key words : Power Management, Discretes, Cellular Phones, High-Power Design, Packaging Techniques, Power Conservation, Reducing Size and Weight, Thermal Management.

Introduction

According to Dataquest (Gartner Group, Inc.), a market research firm, an increase in worldwide cellular/personal communications services (PCS) subscribers, from 203.8 million in 1997 to 647 million in 2002, will drive the handset market from 107.8 million units to 308.0 million units in the same period. Worldwide production of cellular telephone handsets is forecast to grow at a strong 20.7 percent CAGR during the next five years.

Power MOSFETs are the quiet heroes of the current generation of mobile communication systems. In portable cell phones, they are the keys to efficient use of the power from the battery. They are the workers converting the varying battery voltages to the rock-steady voltage required by digital components.

The competitive market for cell phones have compelled manufacturers to always strive for improved battery life, smaller size and more features. Usually at the end of the design chain, the engineers responsible for power management have multiple constraints imposed on each new design which demand smaller packages, and higher currents.

Cellular Phone Power Management Requirements

The cellular phone has to operate for an acceptable amount of time from batteries, so power draw in each component is closely monitored. Each component that is designed into the system has to manage its power, typically through clock switching and powering off. Advances in technology are also driving down the voltage which chips will operate on resulting in significant power savings.

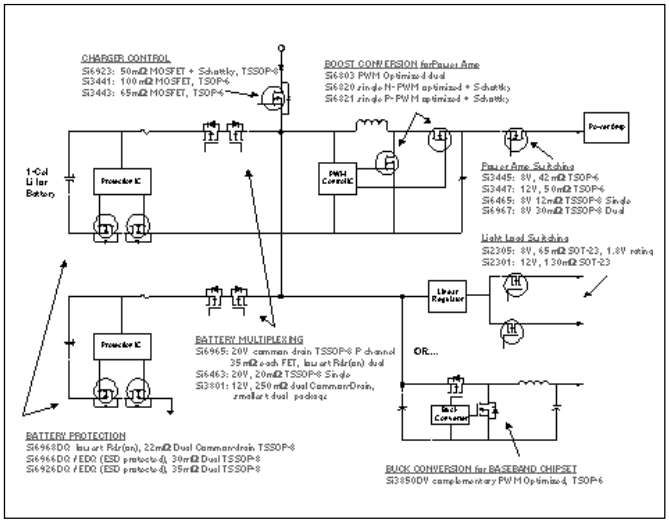

Figure 1. Power Management System in a typical Cellular Phone

The battery pack in the cellular phone will usually contain one to two cells of a rechargeable technology. The battery pack may also contain circuitry to monitor the charge and discharge of the cells to provide an accurate gas gauge so users can stay informed as to the time they have left to operate the cellular phone. Battery technology is slowly increasing in density and weight savings, but silicon advances are happening much faster. Lithium ion is the latest advance in mass produced batteries

and is helping to reduce the weight and keep the same operation time with higher performance systems. Alkaline batteries are much cheaper and more available, but do not have the capacity for the power required for the cellular phone.

The biggest challenge in the cellular phone design was to minimize quiescent current whilst still coping with short term high currents. The typical current being drawn is only tens of milli-amperes, but each supply is required to supply up to 2 amperes. The charging circuit is designed to cope with charging currents of up to two amperes. It is therefore important to minimize power consumption in all situations to maximize battery life.

The aim of power management in the cellular phone is therefore to keep the cellular phone in a fully operational state for as large a proportion of the time as possible. When this is not possible, as when the battery voltage is low, the cellular phone should be in a predictable, low power state. At the same time, power management also means providing the AC to DC voltage conversion as well as the different power rails, typically called DC-to-DC conversion and charging the batteries.

DC-DC Conversion

Low power is essential since battery life is directly related to the power consumed. There are a number of trends that are helping to reduce the power consumption of modern Integrated Circuits (ICs). One is reducing device size, which decreases capacitance and various other parasitic effects, thus reducing power consumption.

A second trend is increased functionality, particularly in chips designed for the embedded environment. A single chip now often includes a number of timers, DMA controllers, a DRAM controller, chip select logic and various ports. The need for off-chip devices is reduced and thus power consumed by the system switching the address and data lines is reduced.

A third trend is lower operating voltage. A system operating at 3.3V will typically consume only about half the power it would at 5V. Some new systems are being designed to operate at even lower voltages than this.

Switch mode converter designers are constantly striving to increase efficiency as well as to decrease overall design volume. One of the ways to decrease the size of any converter is to increase the switching frequency, hence reducing the size of the energy storage elements. Unfortunately the most severe effect of increasing the switching frequency in most topologies is an overall decrease in efficiency, with the most significant loss component being in the MOSFET.

By characterizing the components of loss associated with the MOSFET's switching elements in the cellular phone applications. It will demonstrate the benefits in efficiency, switching speed and delay times of a new family of low on-resistance reduced gate charge MOSFETs.

A simple model of the power loss of a MOSFET used in a dc-to-dc converter (Figure 2) can be calculated if we know the RMS, the current through the MOSFET, the duty cycle, the gate voltage, and the on-resistance of the MOSFET. This model can then be used to compare the efficiency of designs using various MOSFET technologies.

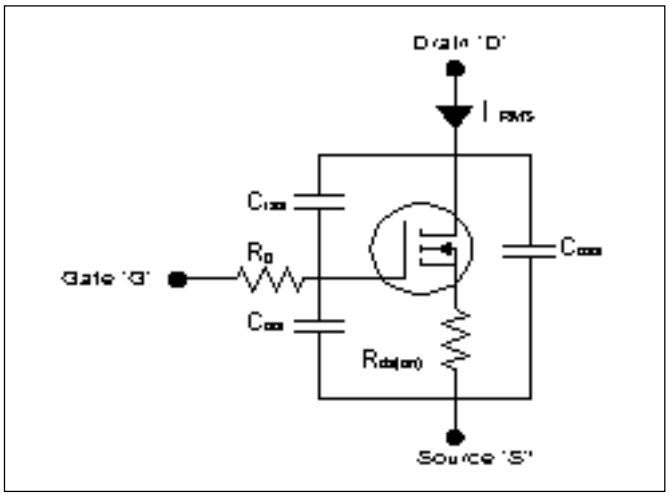

Figure 2. Generic MOSFET model with body diode omitted.

$$P = I^2 RMS \cdot r_{ds(on)} [Vgs][Tj] \cdot D + Qg [Vgs] \cdot Vgs \cdot f \quad Watts \qquad Eq\ 1$$

where

I^2RMS	The RMS current in the MOSFET (A)
$r_{ds(on)}$	On-resistance of the device. (Ohms)
Vgs	The peak gate drive voltage for the MOSFET (V)
[Tj]	Junction temperature of the MOSFET
D	Duty factor of the MOSFET (Ratio of on time to off time)
Qg	Total gate charge for the MOSFET at a given gate voltage (C)
f	Frequency of MOSFET switching (Hz)

Using equation 1 we can obtain a plot of Power Loss (gate loss + $r_{ds(on)}$ loss) as a function of gate voltage at varying switching frequencies (Figure 3).

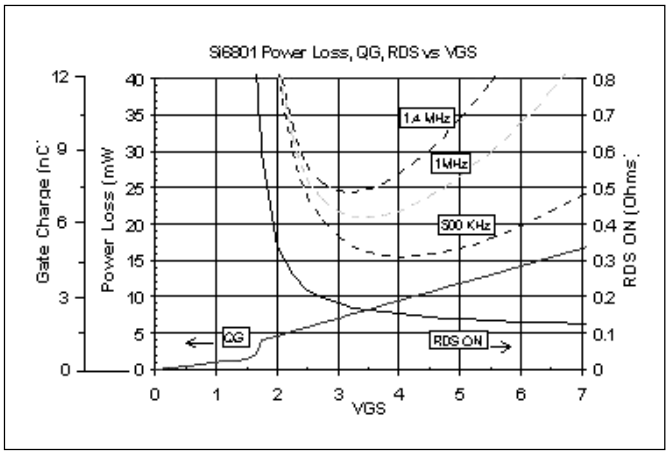

Figure 3. Power loss for PWM optimized Si6801 P-Channel MOSFET as a function of Vgs and switching frequency.

Figure 3 shows the respective contribution of on-resistance and gate charge to overall losses for a p-channel MOSFET at three different switching frequencies. At low gate-source voltages, the $r_{ds(on)}$ of the MOSFET is high and therefore on-resistance losses dominate. At higher gate-source voltages, on-resistance becomes almost a constant and the gate charge losses controlled by Qg dominate. Gate loss increase with the switch-

ing frequency, causing a narrowing in the optimum gate voltage. Therefore, the optimum drive voltage will be at a level, which is just enough to take the $r_{ds(on)}$ into its constant region, but no further. Figure 3 also clearly shows that as switching frequencies increase the loss associated with the gate drive begins to dominate, hence the need for MOSFETs with lower gate charge.

As already stated, reducing the overall gate charge of the MOSFET technology employed will give a significant efficiency benefit. There is a new line of reduced gate charge, fast power MOSFETs or PWM optimized MOSFETs available now. For low voltage DC-to-DC converters two main categories of MOSFETs are optimized: low threshold, 4.5V gate rated planar MOSFET technology, and standard threshold, dense cell trench MOSFET technology, typically used in low power applications and 4.5V gate rated MOSFETs, for higher power converters.

This optimized MOSFET process is suited to low power applications were reduced gate charge is more important than very low on-resistance. Normalized gate charge serves as a quick figure of merit for comparing the PWM optimized, conventional, and low-threshold MOSFETs technologies. This was calculated by normalizing the on-resistance and gate charge of the n-channel MOSFET to 100 mΩ:

Type of MOSFET Technology	Normalized gate charge per 100 mΩ (nC)
PWM optimized Planar	1.4
Conventional Planar	4.0
Low-threshold Planar	22.0

As a first approximation these MOSFETs show a substantial reduction in the gate charge - Rds(on) product. Reducing gate charge is one way in which PWM optimized MOSFETs cut power losses. In a real application, another component of power loss is crossover losses, which is primarily dependent on speed of the switch transition. In the example used here, the Siliconix's Si6801DQ PWM optimized MOSFET is paired with the Si9160BQ switching regulator IC to create a 1MHz synchronous boost converter for cellular telephones. The waveforms measured are between drain and ground of the Si6801DQ MOSFET primary Boost switch. Figure 4 shows oscillograms of the Boost converter switching waveform using the three different types of power MOSFETs comparing different technologies

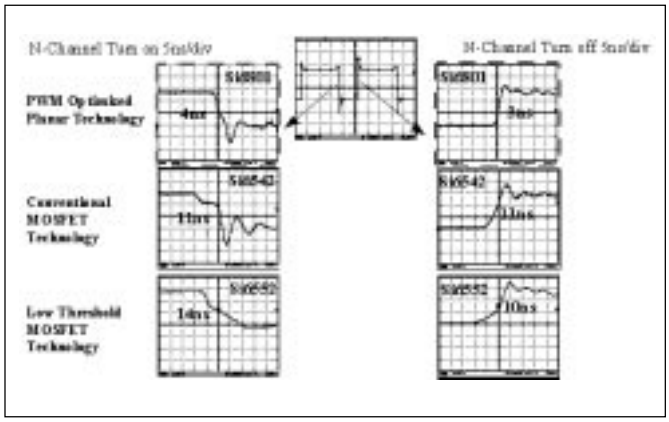

Figure 4. Switching speed comparison between PWM optimized, conventional, and low threshold power MOSFETs.

Switching speeds are 4 ns for the Si6801DQ PWM optimized MOSFET and 11 ns for the conventional MOSFET. The Si6801DQ provides a nearly threefold improvement and thus lower losses. In addition to the increase in basic switching speed, notice that the PWM optimized MOSFET does not exhibit a large characteristic step in the voltage waveform. This step is due to the feedback capacitance from drain to gate of the MOSFET or 'Miller' capacitance being charged when the drain voltage is lower than the gate voltage during a switching transition from an OFF state to an ON state and vice-versa. Effectively the gate voltage is "stalled" while the Miller capacitance is charged, and this is reflected in the voltage waveform from drain to source. In the PWM optimized MOSFET this obviously unwanted characteristic has largely been eliminated.

The overall efficiency increase of the PWM optimized can be seen in figure 5 the three dimensional efficiency Vs switching frequency Vs load current for the chip set combination Si9160 control IC and the Si6801 implementing a Boost converter.

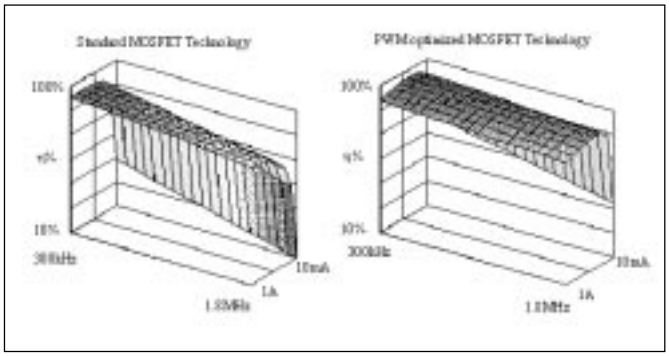

Figure 5. Efficiency comparison between PWM optimized low threshold MOSFET and standard MOSFET technology

Ideally the efficiency would be at 100% at all frequencies and load currents. Note at high loads and lower switching frequencies the optimized technology only gives marginal benefits; however as the switch frequency increases or the load current decreases the lower gate charge, faster switching, devices give a very clear efficiency advantage.

Batteries

Cellular phones draw their power from batteries. The key, therefore, is to manage the battery to achieve the longest possible life while meeting the power requirements. In the cellular phone application, the battery management system comprises the battery, battery charger, battery monitor and system software.

Since their introduction in 1990, Lithium-ion batteries have quickly become the most popular rechargeable battery choice for portable applications. A general rule of thumb is that any portable application that could use NiCd or NiMH battery packs could be better designed with Li-ion. In addition to superior cycle life, lack of voltage depression and low self-discharge advantages of the Li-ion system compared to NiMH, a Li-ion battery pack will provide increased run-time for cellular phones with less weight. Alternatively, one could design a smaller, lighter Li-ion battery pack that provided similar energy to a larger, heavier NiMH pack. With the move to lower total carrying weight for cellular phones, Li-ion battery packs provide significant advantages over other chemistries.

Battery protection

Battery packs include a pair of power MOSFETs that act as a switch to connect or disconnect the battery from the outside world.

Li-ion cells must be designed to safeguard against abnormal charge situations without the aid of external protective mechanisms. Overcharging beyond the upper voltage limit may result in lithium plating and hydraulic pressure generation, cathode instability, electrolyte decomposition and gas generation. Battery pack protection circuitry provides protection against overcharge, over-discharge, over voltage, short circuit and high temperature.

Individual cells are protected against overcharge and over discharge by monitoring the voltage of each cell or set of parallel cells. If any cell exceeds the maximum voltage of 4.25+/-0.05V or drops below the minimum voltage of 2.0+/-0.05V, then the respective charge or discharge will be terminated by switching open a MOSFET.

The components on the pack protection circuitry must be protected against high voltages to prevent their destruction. The pack protection circuitry must be designed to handle excessive voltages or permanently shutdown the battery if a failure occurs. Current flow is monitored to check for unusually high currents, typically created by an external short circuit condition. When encountered, a MOSFET will be opened to stop the flow of current.

Charging

Cellular phones commonly have internal power supplies that provide a charging supply to the cellular phones while the battery is connected to the device. There are two charging schemes, which can be employed to charge Li-ion batteries : constant current/constant voltage and pulsed constant current.

The standard charging technique for Li-ion batteries is a constant current limited charge to an upper voltage followed by a constant voltage charge, terminated either by time and/or minimum charge current value. In this method, the time to reach full charge is less than optimum.

The pulsed constant current charge method, on the other hand, allows a simple charger to output constant current to charge either NiCd, NiMH or Li-Ion battery packs, as the charge control is done inside the battery pack. Each battery type would control the same constant current source differently to perform a complete and safe charge. Siliconix's Si9730DY is a pack protection IC with a very small hysteresis. The IC is designed for overcharge and over discharge protection. When used for charge control, one level of redundant safety is lost. As a result, it is used with a microprocessor to monitor individual cell voltages to provide the extra level of overcharge protection that was lost when the pack protection IC was used for charge control.

Dual battery systems

Another similar application is to switch between batteries on the input of the DC/DC converter. This is useful if the cellular phone has removable battery packs and it is designed to work while the battery packs are being changed.

MOSFETs are often used with Schottky diodes for power switching: in cell phones, for example, to disconnect the battery when the power is supplied from the cigarette lighter cable, or in other portable devices where two alternative power sources exist. Here the Schottky diode is needed to overcome the MOSFET's internal diode, which can conduct when the MOSFET is off. By putting the Schottky in series with the MOSFET, the internal diode is, in effect, eliminated, creating a simple reverse blocking switch (Figure 6). The important specifications for this MOSFET/Schottky device are more obvious than in the other examples. On-resistance is much more important than gate charge for this application, as the MOSFET will not be switching at a high frequency. For this reason, the Si6923DQ has about one-quarter the on-resistance of the otherwise similar Si6821DQ, reflecting its optimization for power routing applications. On first examination, the Si6923DQ could be used for DC-DC conversion. But in practice the Si6821DQ would give higher efficiency in a DC-DC converter despite its higher $R_{DS(on)}$.

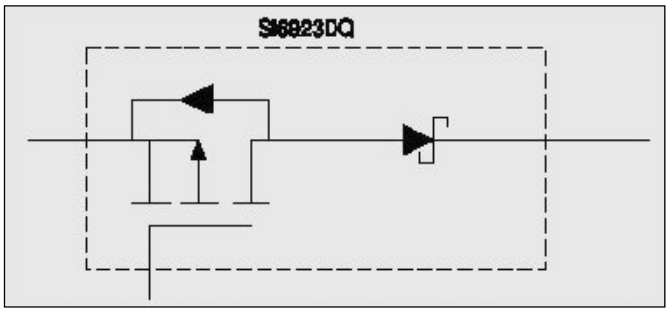

Figure 6 Siliconix's Si6923DQ optimized as a reverse blocking switch

Since such a circuit requires two active devices, the space requirement can be significant. In the circuit shown below, Figure 7, the discrete Schottky and MOSFET are replaced by a dual MOSFET residing on a single chip and packaged in a TSOP-6 with a 2.7 x 2.9 mm footprint only slightly larger than the area of the active silicon. Since the MOSFETs are packaged back to back, they replace the MOSFET plus Schottky configuration usually used for switching between power supplies. Since the loads in these power switching circuits are usually below one amp, the dual MOSFET solution compares very favorably in voltage drop with a discrete MOSFET and Schottky as well as with combination devices in much larger packages.

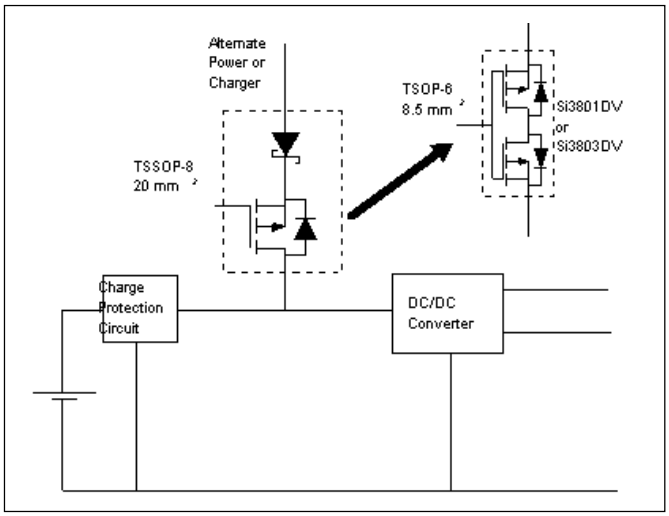

Figure 7 A TSOP-6 Dual MOSFET Battery Switch replaces a MOSFET and a Schottky Diode

The Si3801DV contains two MOSFETs connected together in series. The reason for connecting two MOSFETS together

like this is to ensure that the internal diode, which is an integral part of every MOSFET, does not conduct electricity when the device is off. This configuration thus allows the Si3801DV to be used as a switch in applications where current could possibly flow both ways.

Load switching

A typical power management unit allows the designer, via software, to control the peripherals from halt to full speed operation.

The switching of power to various sections of the cellular phone is performed using power MOSFETs as switches. In most cases N-channel MOSFETs are used together with low power high-side FET drivers. The advantages of using N-channel rather than P-channel FETs include lower cost, a wider range of devices and the ease with which they can default to "open" on power up.

However, the P-channel MOSFET provides the simplest solution for a high-side load switching. Unlike load switches using N-channel devices, there is no need for other voltages or charge pump circuits to provide proper gate-to-source voltages. Also, advances in silicon technology have minimized the cost differential between N-channel and P-channel MOSFETs.

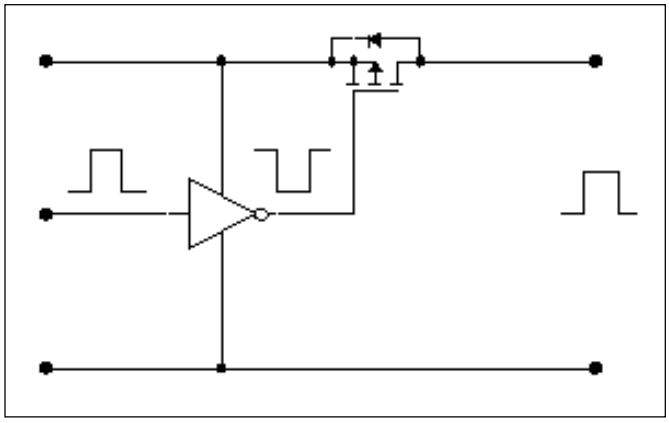

Figure 8 Basic P-channel Load Switch

Figure 8 shows a basic P-channel load switch. The source is connected to the bus voltage while the drain is connected to the control circuit. The control circuit must provide sufficient gate-to-source voltage to ensure a fully enhanced turn on and a discharge path to ensure full turn off. Since the MOSFET is a P-channel, the gate voltage must be negative with respect to the source.

The control circuit can be as simple as a logic gate or it may be a simple network of resistors, capacitors and small signal transistors. The determining factors are the voltage of the bus being switched, the maximum Vgs of the MOSFET and the desired switching speed for the switch. The simplest circuit is when the bus voltage is less than the absolute maximum value of the Vgs. The inverter circuit as shown in Figure 8 can be nothing more than a small signal N-channel MOSFET that pulls the gate to ground as shown in Figure 9 below. The gate-to-source resistor provides the discharge path required for the MOSFET to turn off.

If the switching time needs to be slower to perform a function such as limiting inrush current, the gate resistance and external gate-source capacitance can be added as shown in Figure 10. When Q1 turns on, the gate capacitance and external capacitance is charged through RG. The gate-to-source voltage

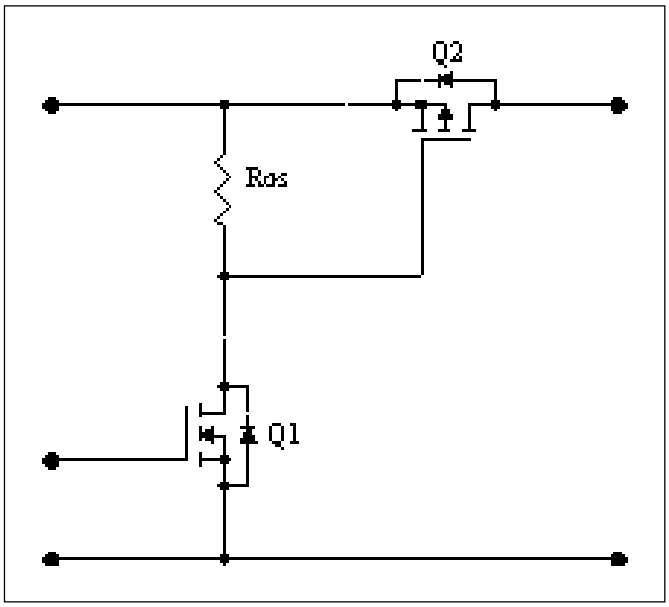

Figure 9 Basic P-Channel Load Switch utilizing a small signal N-Channel MOSFET

will increase according to the R-C time constant until it reaches the voltage defined by the voltage divider as created by RGS and RG. This voltage must be compatible with the MOSFET's RDS(on) rating to ensure that the MOSFET turns on fully.

To speed up the turn off while maintaining the slow turn on of Figure 11, an extra small signal MOSFET and two resistors must be added as shown in Figure 11. This P-channel MOSFET is turned on when the load switch is turned off, shorting the load switch's gate to its source therefore turning off the load switch quickly.

Finally, when the bus voltage exceeds the absolute maximum Vgs, the basic circuit must have a voltage divider on the gate to ensure that the Vgs specification is not violated. This function is performed by the resistive divider formed by Rg and Rgs in Figure 10 and 11.

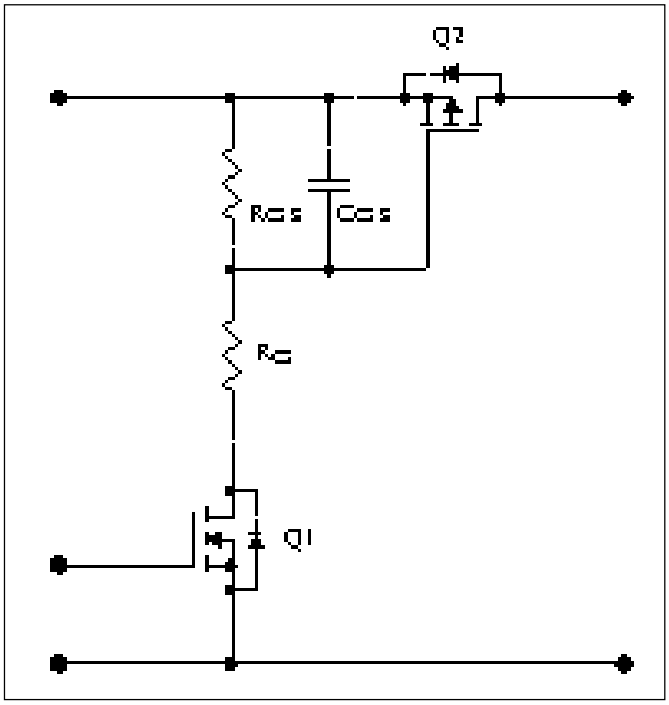

Figure 10 P-Channel Load Switch with reduced switching speed

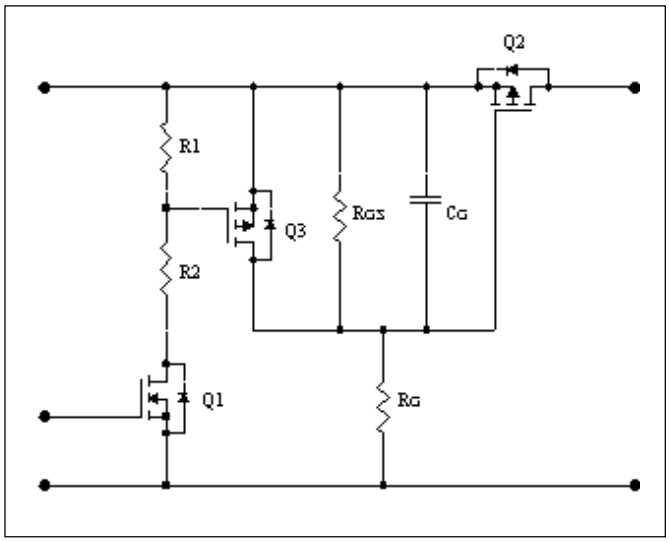

Figure 11 Full featured P-Channel Load Switch

What are MOSFETs ?

Power MOSFETs are renowned for two important features: low Rds(on) and simple gate drive requirements. MOSFETs are bi-directional, which means that the low Rds(on) is exhibited with both positive and negative drain currents. However, the reverse characteristics are normally dominated by a parallel diode, which is part of the MOSFET structure and is capable of carrying significant currents. This bi-directional property is very useful in applications that require reverse blocking capability, such as synchronous rectification. Using the MOSFET with a negative drain current allows the MOSFET to block in the reverse direction, but the voltage drop across the device will still be governed by the Rds(on) rather than the diode forward drop.

Power MOSFET packaging has evolved from the TO-220 through-hole package, the industry standard workhorse, to the surface-mount D2PAK. In 1990, Siliconix revolutionized the industry with the introduction of the first Power MOSFET in the small-outline 8-lead package.

Before selecting a MOSFET, several circuit parameters must be defined. They are the bus voltage, load current, maximum allowable voltage drop across switch and the maximum ambient temperature. Once these circuit parameters are known, four specifications must be considered - Vds, Vgs, Rds(on) and Rθja.

The Vds of the MOSFET selected should provide about 25% headroom above the bus voltage being switched. The value of the Rds(on) along with the maximum current through the switch determines the voltage drop across the switch and the power dissipation of the switch. When evaluating the voltage drop and power, this value should be the maximum value of the Rds(on) compensated for a junction temperature of 150ºC. The drive method must not exceed the absolute maximum of the Vgs. This can occur when the bus voltage is greater than Vgs. Finally the Rθja of the MOSFET package must be evaluated to ensure that the package can dissipate the conduction losses of the switch.

Summary

Reduced gate charge MOSFETs, with improved switching performance, are an enabling technology that allow the DC to DC designer to either increase efficiency or switching frequency to suit the design goals.

One approach to improving the efficiency of DC-DC conversion and power routing circuits in portable systems is to tailor the MOSFET characteristics to the specific application. However, merely adding new features or integrating other parts of the circuit does not automatically make a useful product. To make the product useful, the needs of the application must be understood and the product must be optimized for that application. The new family of LITTLE FOOT Plus MOSFETs is an example of application-specific power semiconductors that will simplify designs, increase higher frequency topologies and reduce component count.

This new family of MOSFETs is the next step in application-specific power semiconductors. Each device is optimized for a specific application and excels in that application. All electrical, mechanical and thermal parameters have been considered for each device. The devices in this family combine super low on-resistance with added features. This philosophy of application-specific optimization will be continued to produce more devices in this family that will simplify designs and increase efficiency of power conversion and power routing in battery operated equipment.

The TSOP-6 PowerConnect packaged Si3081DV provides the reverse-blocking function in much less space and with lower component count than the typical solutions of a larger packaged dual MOSFET or a MOSFET in series with a Schottky diode. The applications for such devices are diverse, as they approach the long sought after goal of eliminating the parasitic diode. This solution is the first in a TSOP-6 and carries a lower price tag than previous solutions using IC technology to eliminate the diode. The Si3801DV will allow manufacturers to provide the availability of long talk times, the option of going "lightweight", more affordably, and with less board space, than was ever before possible.

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