Signal integrity: Ensuring reliability in today's digital designs

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Signal integrity is a broad topic, one that impacts many electronic design disciplines. But until a few years ago, it wasn't much of a problem for digital designers. They could rely on their logic designs to act like the Boolean circuits they were. Noisy, indeterminate signals were something that occurred in high-speed designs-something for RF designers to worry about. Digital systems switched slowly and signals stabilized predictably.

Market forces in the PC, networking, and telecommunications realms have changed everything, following a curve on which the pace of change itself is accelerating. Processor clock rates have multiplied by orders of magnitude. Computer applications such as 3D graphics, video, and server I/O demand vast bandwidth. Much of today's telecommunications equipment is digitally based, and similarly requires massive bandwidth. So too does digital high-definition TV.

At the functional circuit level, the term "bandwidth" means speed-high data rates, narrow pulses, and fast rise/fall times. Integrated circuit processes have evolved, generation by generation, to meet the market's speed demands. The current crop of microprocessor devices handles data at rates up to 2, 3 and even 5 gigabytes per second (GB/s), while some memory devices use 400-MHz clocks as well as data signals with 200 ps rise times.

Importantly, speed increases have trickled down to the common IC devices used in automobiles, VCRs, and machine controllers, to name just a few applications. A processor running at a 20-MHz clock rate may well have signals with rise times similar to those of an 800-MHz processor. We have crossed a performance threshold that means, in effect, almost every design is a high-speed design.

Without some precautionary measures, high-speed problems can creep into otherwise conventional digital designs. If a circuit is experiencing intermittent failures, or if it encounters errors at voltage and temperature extremes, chances are there are some hidden signal integrity problems. These can affect time-to-market, product reliability, EMI compliance, and more.

It's time to face signal integrity problems head-on.

Why is Signal Integrity "Suddenly" a Problem?

Let's look at some of the specific causes of signal degradation in today's digital designs. Why are these problems so much more prevalent today than in years past?

The answer is, again, speed. In the "slow old days," maintaining acceptable digital signal quality meant paying attention to details like clock distribution, signal path design, noise margins, loading effects, transmission line effects, bus termination, decoupling, and power distribution. All of these rules still apply, but...

Bus cycle times are up to a thousand times faster than they were 20 years ago! Transactions that once took microseconds are now measured in nanoseconds. To achieve this improvement, edge speeds too have accelerated: they are up to 100 times faster than those of two decades ago.

This is all well and good; however, certain physical realities have kept circuit board technology from keeping up the pace. The propagation time of inter-chip buses has remained almost unchanged over the decades. Geometries have shrunk, certainly, but there is still a need to provide circuit board real estate for IC devices, connectors, passive components and of course the bus traces themselves. This real estate adds up to distance, and distance means time-the enemy of speed.

The ratio of device rise time to circuit board propagation delay has changed by about two orders of magnitude over the last 20 years. Even a system that doesn't use the latest 1 GHz processor may be populated with, say, 50-MHz devices whose rise time pushes the limits of printed circuit trace technology. It's important to remember that the edge speed-rise time-of a digital signal can carry much higher frequency components than its repetition rate might imply. For this reason, some designers deliberately seek IC devices with relatively "slow" rise times.

The lumped circuit model has always been the basis of most calculations used to predict signal behavior in a circuit. But when edge speeds are more than four to six times faster than the signal path delay, the simple lumped model no longer applies.

Circuit board traces just six inches long become transmission lines when driven with signals exhibiting edge rates below four to six nanoseconds, irrespective of the cycle rate. In effect, new signal paths are created. These intangible connections aren't

on the schematics, but nevertheless provide a means for signals to influence one another in unpredictable ways.

At the same time, the intended signal paths don't work the way they are supposed to. Ground planes and power planes, like the signal traces described above, become inductive and act like transmission lines; power supply decoupling is far less effective. EMI goes up as faster edge speeds produce shorter wavelengths relative to the bus length. Crosstalk increases.

In addition, fast edge speeds require generally higher currents to produce them. Higher currents tend to cause ground bounce, especially on wide buses in which many signals transition at once. Moreover, higher current increases the amount of radiated magnetic energy and with it, crosstalk.

What do all these characteristics have in common? They are classic analog phenomena. To solve signal integrity problems, digital designers need to step into the analog domain. And to make that step, they need tools that can show them how the digital and analog worlds interact.

Viewing the Analog Origins of Digital Signals

The long-established solution for digital design verification and troubleshooting work is the logic analyzer. There is simply no better tool for capturing and analyzing timing relationships, logic state activity, and software execution steps. A logic analyzer such as the Tektronix TLA600 or TLA700 Series can capture many thousands of cycles of bus activity and display waveforms and code symbols for each.

Equally important, the logic analyzer can trigger on numerous conditions, including digital errors of various types. The logic analyzer is a tool that can help you quickly pinpoint digital faults in your design.

But these digital errors often have their roots in analog signal integrity problems. To track down the cause of the digital fault, it's often necessary to turn to an oscilloscope, which can display waveform details, edges, and noise; can detect and display transients; and can help you precisely measure timing relationships such as setup and hold times.

Compare the two waveform traces in Figure 1. The upper trace is the purely digital signal the logic analyzer sees. The lower trace is an oscilloscope's view of the same signal. An engineer examining this display would immediately recognize the analog aberrations that caused the "false" transition in the digital signal.

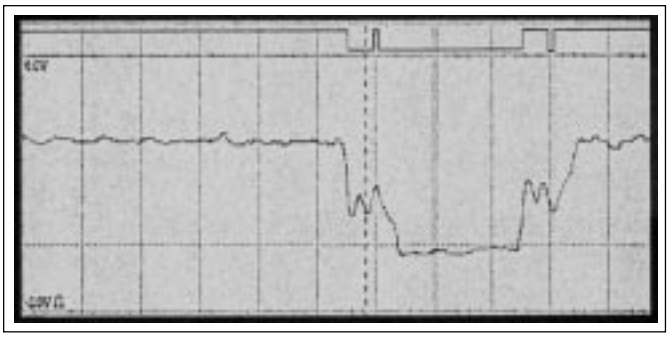

Figure 1: Time-correlated digital and analog signal views

Clearly the solution to digital signal integrity problems requires both logic analyzer and oscilloscope functions. For years, engineers have used the two discrete instruments in tandem, first detecting a digital fault with the logic analyzer, then using their knowledge of that fault to set up the oscilloscope's trigger to capture the same event. Of course, this approach requires a consistent, repetitive event. If the problem is intermittent or aperiodic, then it is very difficult to capture reliably. And the two waveforms don't co-exist on the same display, complicating the effort to interpret their timing relationships.

A workable solution emerged in the form of cross-triggering features built into compatible logic analyzers and oscilloscopes. While this simplified the simultaneous capture problem (by ensuring that the DSO responded to the logic analyzer trigger), it did not address the need to display both waveforms on a single screen.

Signal Integrity Solutions

The need for an effective integrated logic analyzer/oscilloscope solution has not gone unnoticed by instrumentation vendors. Several alternatives have emerged over the past few years, each with its strengths. Each solution allows users to trigger on a digital problem (that is, detect it) and capture the related analog waveform information simultaneously.

The alternatives differ in their cost and flexibility, but all of them offer the ability to display, on one screen, time-correlated waveforms from the two domains-analog and digital. There are three basic architectures that segment the logic analyzer and oscilloscope functions in different ways:

1. The modular logic analyzer with integral plug-in DSO modules
2. The non-modular, monolithic logic analyzer/DSO combination
3. The fully-integrated pairing of discrete logic analyzer and DSO instruments

The Modular Approach

The first truly integrated, high-performance logic analyzer/DSO solution was the Tektronix TLA700 Series, a modular logic analyzer family with plug-in DSO modules. The instrument is an uncompromised logic analyzer built on a mainframe concept that allows either digital or analog modules to plug into the system. The available DSO is a powerful 2- or 4-channel unit with 500-MHz or 1-GHz bandwidth. They provide a full array of oscilloscope functions, and is specifically designed to accept a trigger command from the TLA700 Series' logic modules via internal high-speed signals. The oscilloscope module's acquisition data is stored in the module's own 15,000-sample memory, and is automatically time-correlated with the logic analyzer data captured when a trigger occurs. The results from both instruments are displayed on the TLA700 screen.

The modular logic analyzer delivers the valued benefit of configurability. On the digital side, it gives users the opportunity to configure as many digital channels as they need (into the hundreds), to handle growing numbers of buses and device pins. Oscilloscope capability, too, is configurable in terms of bandwidth - up to 1-GHz maximum at 5 gigasamples per second (Gs/s) - and channel count. The modular system requires no special cabling between the logic analyzer and the oscilloscope.

Modular solutions have their limitations. High-performance oscilloscopes or advanced features are not always readily available, restricting a user's ability to use the integrated solution to its maximum performance potential. In addition, some designers may require a separate oscilloscope to enable individual oscilloscope-based test needs, driving up the total investment in bench-top instrumentation.

The "Fixed-Configuration" Solution

Fixed configuration tools offer innate simplicity and the

convenience of a compact, self-contained benchtop instrument. Within their performance limits, they are a cost-effective way to bring digital and analog waveforms into the same environment. They can offer the same efficient level of integration as the modular system described above.

Fixed-configuration systems, however, are bound by the specifications of the two built-in "instruments" they encompass. The target application must not exceed either the digital pin count or the analog bandwidth of the integrated instruments. Some advanced features are not available in the built-in oscilloscope, which means a separate instrument must be purchased for many oscilloscope measurements.

The fixed-configuration tool is limited to the capabilities it was built with. As the target application evolves (inevitably requiring higher speeds, or more channels, or both), the instrument can't evolve with it. In addition, when using this configuration, the oscilloscope is not available for use by other team members. Still, the fixed logic analyzer/oscilloscope may be the lowest-cost answer if the target requirements are within its reach and expected to remain stable for the life of the instrument.

The Integrated Instrument Pairing

Many digital design applications require a solution that can deliver an optimum balance of logic analyzer and oscilloscope features today, and grow with changing measurement needs. Most leading instrument makers already have a broad range of logic analyzer and oscilloscope models, reflecting diverse performance and price levels. Why not develop a solution that lets users pick and choose the exact combination of digital and analog attributes they need? If users have the means to quickly set up, acquire, transfer, and time-correlate oscilloscope waveforms on a logic analyzer, they will have the best of both worlds.

That is the rationale behind the latest class of solutions to reach the market. The integrated instrument pairing is the most open of the three approaches discussed here. Importantly, the term "pairing" doesn't imply matching a specific logic analyzer with a specific oscilloscope model. In a sense, the integration itself is the solution, while the instruments are the flexible components you choose according to your application needs.

The instrument pairing architecture is built around a software and interconnect package that seamlessly integrates proven logic analyzers and oscilloscopes, creating an interoperable tool set for digital development and troubleshooting.

Tektronix' Integrated View (iView) capability integrates the company's TLA600 or TLA700 Series logic analyzers with external oscilloscopes in the TDS3000 Series, as well as the high-performance TDS7000 Series and TDS684C/694C oscilloscopes. The solution makes it possible to transport oscilloscope waveforms to the logic analyzer display and automatically time correlate them. The two types of waveforms can even be superimposed if desired.

With the paired instrument approach, users can match virtually any digital performance level to an equally broad analog performance range. For example, designers developing a server with the fastest, most complex processors and buses will want high channel count, bandwidth, and memory depth on the digital side, and exceptional acquisition (sample) rate on the analog side. These engineers might combine a TLA700 logic analyzer with a 4-GHz TDS7404 Series oscilloscope.

In contrast, a design team working on an automotive drive-by-wire controller may require fewer digital channels and generally lower bandwidth. They might choose a smaller TLA700 Series logic analyzer configuration or its self-contained equivalent, the TLA600 Series. They might then match this digital toolset with a cost-effective 500-MHz TDS3000 Series digital phosphor oscilloscope.

It's worthwhile to note that the paired instrument approach overcomes the record-length limitations that exist in the other configurations. In the past, logic analyzers' record length has far exceeded that of any oscilloscope that could be integrated. With the much broader choice of models available for the paired instrument user, the oscilloscope can be chosen to better match the amount of "time" the logic analyzer can record.

Summary

High-frequency design concepts are no longer something the digital hardware engineer can afford to ignore. With today's digital devices producing sub-nanosecond rise times and clock rates exceeding 1 GHz, the digital designer is as likely to run into signal integrity problems as is the RF engineer.

At speeds in the GHz range, circuits begin to exhibit increasing crosstalk, noise, jitter, EMI, and more. These signal integrity problems can be traced to the growing gap between conventional circuit board performance and present-day IC clock and edge rates.

Troubleshooting signal integrity problems requires careful attention to the analog characteristics of digital signals, and this in turn calls for an integrated measurement solution that can capture and display both domains in one time-correlated view.

Today, engineers can choose from several solutions, all of which integrate the features of a logic analyzer with those of an oscilloscope. The choice depends on many variables: the required mix of analog and digital capabilities, cost, anticipated need to expand analog or digital functionality, and more. Increasingly, designers are looking for flexible solutions that they can configure for their specific bandwidth, channel count, and record length needs. The integrated instrument pairing is a promising new solution to this requirement.

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Agenda

- Confronting Signal Integrity Issues In Everyday Digital Design Work
- Why is Signal Integrity "Suddenly" a Problem?
- Viewing The Analog Origins of Digital Signals
- Signal Integrity Solutions
- Summary

People are talking about *Signal Integrity*

"There are two kinds of designers, those that have signal integrity problems, and those who will."
– *Sun Microsystems*

"...as everyone knows, intermittent quality problems mean almost certain death in today's competitive marketplace."
– *Greg Doyle, Mentor Graphics*
Rod Strange, SiQual, Inc.

"Faced with killer schedules and extremely complex designs, engineers are reluctant to even think about signal-integrity issues. But with system speeds getting faster, these problems are going to become an everyday occurrence for engineers."
– *Rod Strange, SiQual, Inc.*

Digital Signal Integrity Defined

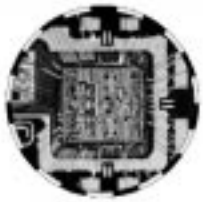
- *Digital signal integrity is all about distributing signals from one part of a digital circuit to another in a way that deterministically and dependably delivers the digital information contained therein.*
- Ensuring adequate Digital Signal Integrity requires specific analysis in the design phase and characterization by empirical measurements of prototypes to validate the effectiveness of the design modeling methods.

Digital Signal Integrity Defined

- The goal is to ensure flawless operation with sufficient design margins to accommodate realistic variations in:
  - **Device characteristics**
    - edge rates
    - timing margins
    - voltage margins
  - **Operating conditions**
    - supply voltage
    - clock frequency
    - temperature & other environmental factors
  - **Manufacturing process**
    - ECB trace & stackup geometries
    - component placement accuracy & soldering

Debug Challenges

- Does the design work?
- Does the design always work under all conditions?



Why is This Such a Big Deal Today?

- ***Market Forces Drive Technology Trends*** - applications require more digital data bandwidth
- ***Bandwidth Demands Push Edge Rates*** - faster edge rates make signal integrity an issue where it once was not
- ***Semiconductor Evolution*** - signal edge rates are faster whether they need to be or not!

Market Forces - Digital Data Bandwidth

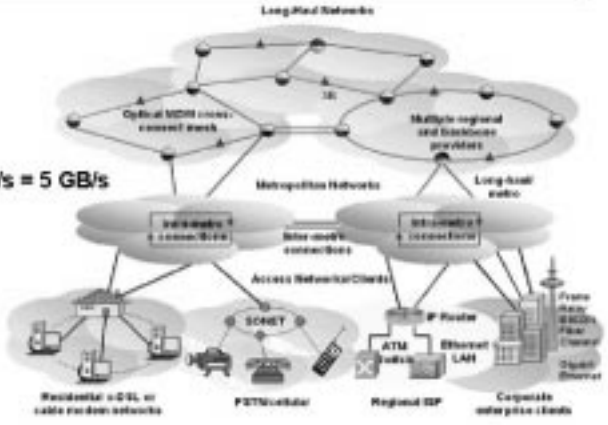
- *Pentium 4 - >1GHz, 400MHz bus, 3.2GB/s bus transfer rate (IDF August 2000)*
- *"The 21264 ...channels up to 5.3 Gbytes/s of cache data ...into the processor, feeding its demanding CPU core." (Compaq web site on Alpha 21264 RISC processor)*
- "Peak Memory BW (2.13 GB/sec)" *(IBM web site regarding RS-6000 RISC processor)*
- "The PCI (Peripheral Component Interconnect) bus provides data rates of one GByte per second and up" *(Intel web site)*

Market Forces -- Computer Systems

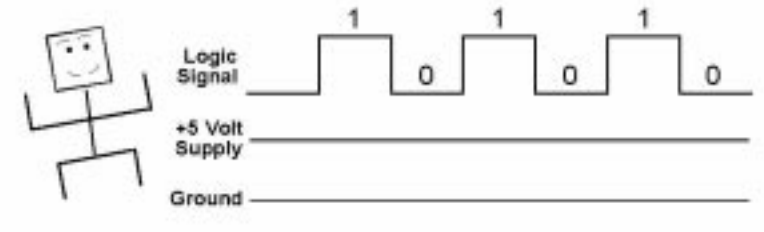
- 3D Graphics
- Digital imaging
- Video
- Server IO

Market Forces -- Communication Infrastructure

- OC-12
- OC-48
- OC-192
- OC-768
  - 40 Gb/s = 5 GB/s

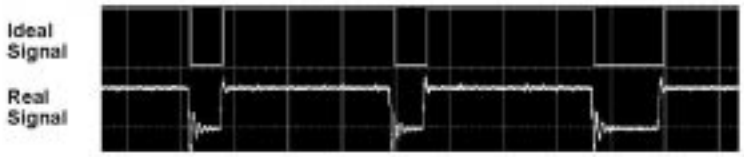


Ideal View of Digital Signals



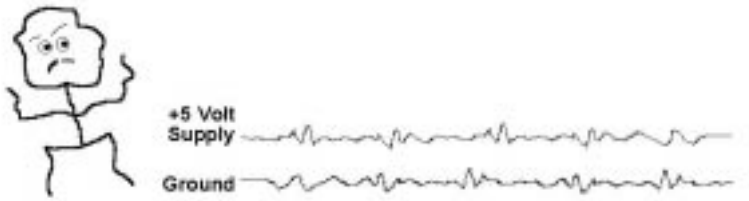
Real View of Digital Signals

Digital Signals Have Complex Analog Attributes



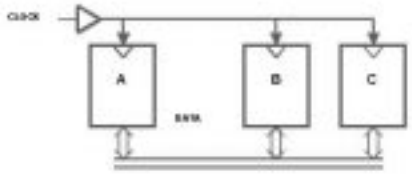
- They result from the complex interactions of characteristics of various circuit elements.
  - The output drivers
  - The layout of the signal distribution path
  - Any loads on the signal path
  - Signal path termination

Power and Ground Lines are Affected Too



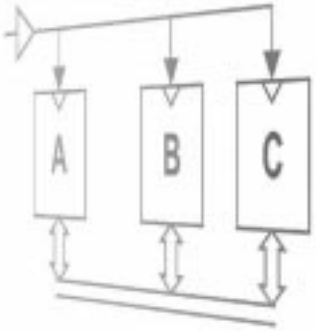
Digital Signal Integrity Problems

- Ringing
- Reflections
- Overshoot & Undershoot
- Glitches
- Clock Skew
- Jitter
- EMI
- Ground bounce
- Power supply noise
- Crosstalk



Design Issues for Digital Signals

- Clock distribution
- Signal path design
  - Transmission line effects
  - Termination
  - Stubs
  - Load analysis
  - Signal path return currents
- Noise margin
- Decoupling
- Power distribution design



Faster Edge Speeds

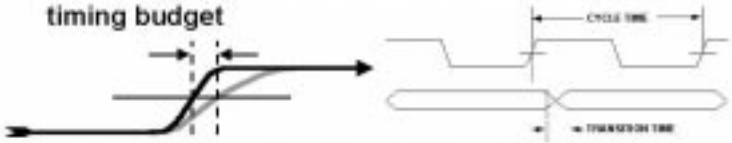
- Rambus 200ps rise/fall times
- DDR <250ps
- Firewire 1394b 80-300ps
- USB2 <500ps
- InfiniBand <100ps

RAMBUS

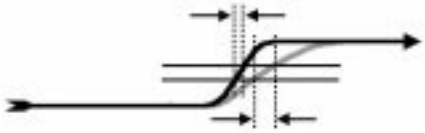
FireWireStuff
IEEE 1394

The Benefits of Faster Edge Rates

- Faster edge speeds can leave more time in the timing budget

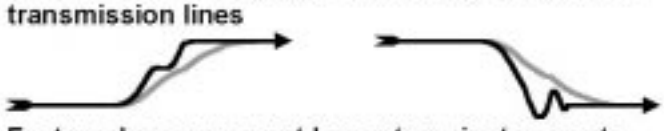


- Faster edge speeds reduce timing differences caused by logic threshold variations



The Cost of Faster Edge Rates

- Faster edges turn lumped circuit trace loads into transmission lines



- Faster edges represent larger transient currents
  - increased ground bounce, especially on wide buses

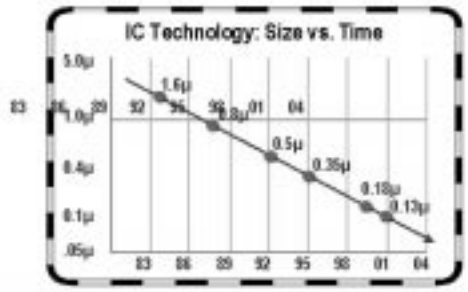
  - increased crosstalk
- You often can't buy parts with slower edges!

The Cost of Faster Edges

- Edge speed (or risetime) represents the frequency components of digital signals
- Circuit modeling becomes dramatically more complex as frequencies rise
  - New signal paths appear (that are not in schematics)
  - Old ones fail to work – old rules for decoupling devices fail with faster edges because the planes that connect them become inductive or transmission lines
  - Electromagnetic emissions increase as faster edges produce shorter wavelengths relative to the bus length
  - Crosstalk increases with faster edges

Semiconductor Evolution

- "Every time an IC vendor optimizes their process or moves to a new process generation and shrinks the die, the rise time will get shorter and signal integrity problems will increase." Eric Bogatin, "Signal Integrity Corner"



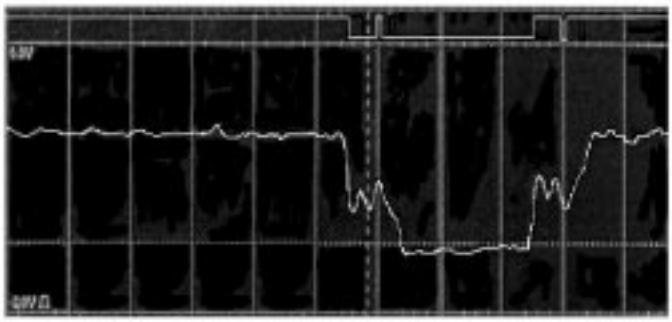
Evolution of Board Layout Technology

- Connecting the dots
- Simulation of worst-case device delays and run lengths
- Careful layout of clock distribution paths and a few fast signals
- Full-scale analog simulation of entire high-speed buses with complex models of:
  - Drivers
  - Receivers
  - Termination
  - Connectors
  - Every pad, via, lateral span, and corner of each run.

Board Layout Challenges

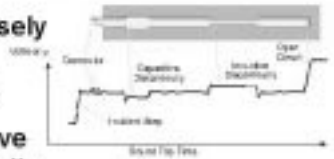
- Signals are affected by many AC components that are not on the schematics
- Adjacent run and plane proximity
- Ground noise - from ground return currents and lack of decoupling
- Transmission line effects

Board Layout Challenges



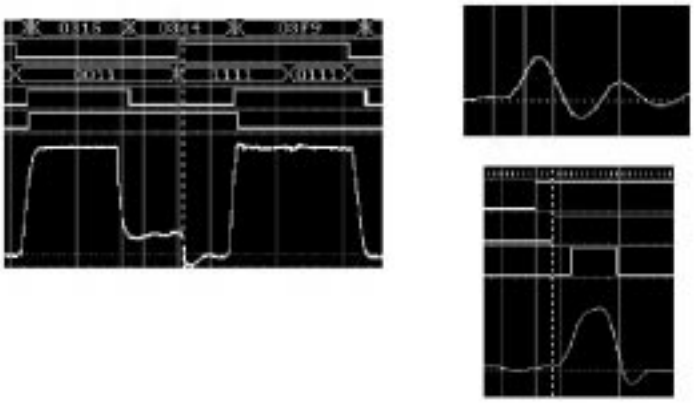
Board Measurement Considerations

- Use TDR capabilities to precisely characterize signal paths (while they are not operating)

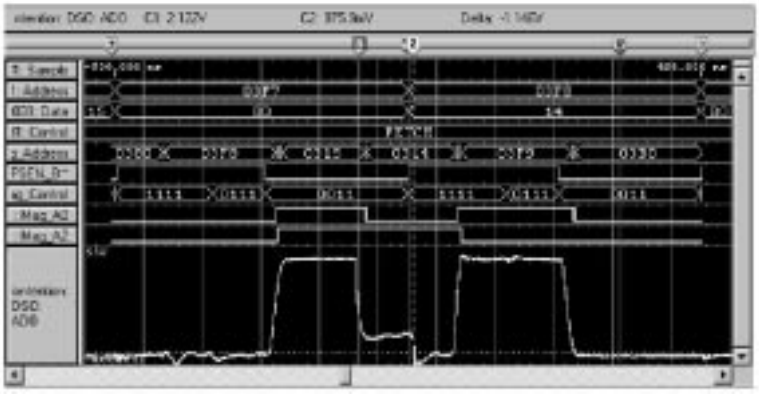


- Use an oscilloscope to observe signal path characteristics while operating under typical conditions
  - Requires sufficient BW to view transmission line effects
- Use Logic Analyzer and Oscilloscope together to relate specific signal phenomenon to digital behavior

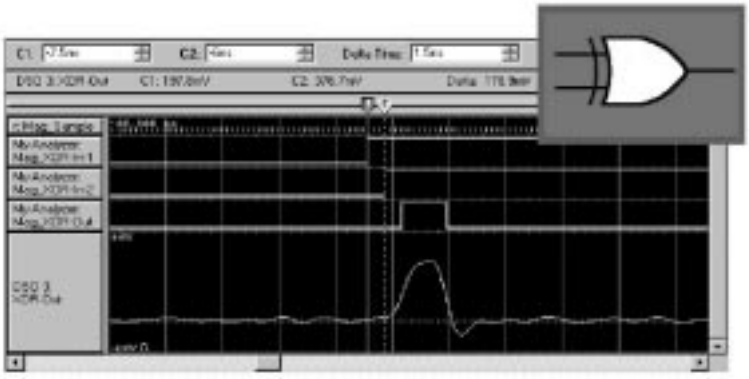
Signal Integrity Anomalies Can Also Be Caused by Functional Problems



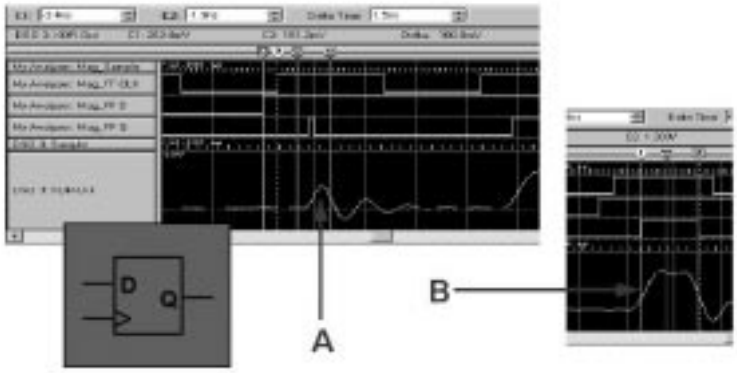
Signal/Bus Contentions



Race Conditions



Metastable Latched Outputs



Digital Applications Have Lots of Signals

- Use a Logic Analyzer to acquire logical operation of the digital system
- Use a Logic Analyzer to acquire detailed timing of the digital signals
- Use an Oscilloscope or a DSO module in the logic analyzer to see individual signal quality
  - Requires full bandwidth & sample rate for single-shot use
- Cross-trigger and view correlated data

Key Market Research Findings

- Screener survey of Logic Analyzer users, done internationally with a sample of 908.
- Users were asked, "During the past 12 months, did you at any time use an oscilloscope *with* a logic analyzer?"

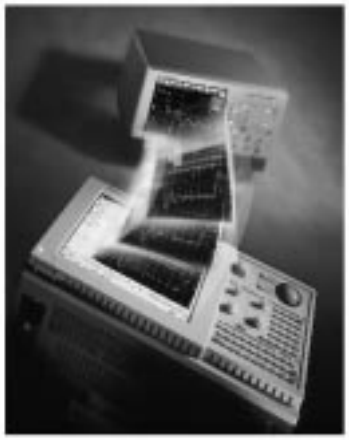
Uses Scope w/Logic Analyzer	
United States **91%**	Great Britain **93%**
Germany **86%**	Taiwan **93%**

Among Those Who Said "Yes"	
61%	used a standalone oscilloscope
23%	used a DSO integrated into a Logic Analyzer
16%	used both

Advanced Triggering Capabilities To Consider

- Oscilloscope triggering
  - Edge (Level, Slew Rate)
  - Pulse (Width, Glitch, Runt)
  - Setup-and-hold time
  - Logic (And, Or, Nand, Nor)
    - Timing (4 Channels) or State (3 Channels + 1 Clock)
- Real-time triggering on setup-and-hold violations and glitches across hundreds of channels simultaneously
- Logic-Analyzer-to-Oscilloscope cross triggering and correlation

Signal Integrity Debugging with Integrated View



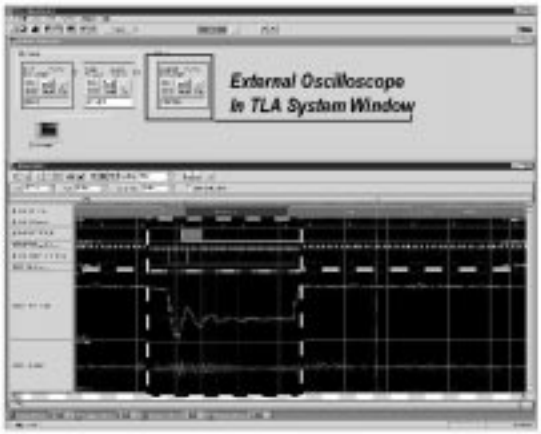
NEW iView (Integrated View)

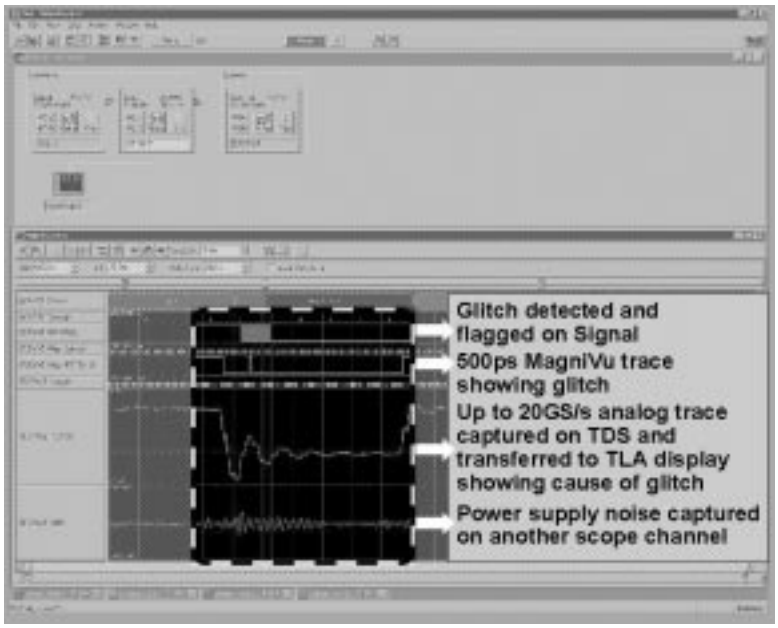
- New capability that provides an integrated view of analog signals from a TDS oscilloscope and digital logic signals and embedded software from a TLA logic analyzer on the same logic analyzer display

iView Integrated View

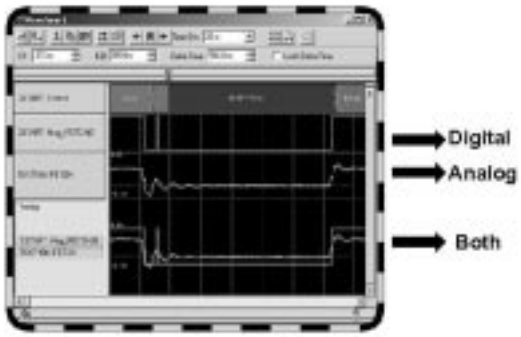
- Makes combined Analog/Digital measurements easy to obtain *at the time they are needed*
- Logic Analyzer automatically retrieves, correlates, and displays Oscilloscope data
  - Just like internal Oscilloscope modules
- Flexible Cross-triggering
  - Logic Analyzer triggers Oscilloscope
  - Oscilloscope triggers Logic Analyzer
  - Independent triggering
  - System trigger tool makes setup easy
- One button starts both instruments
- Instruments can still easily be used independently

Analog And Digital Signals Share The Same Display



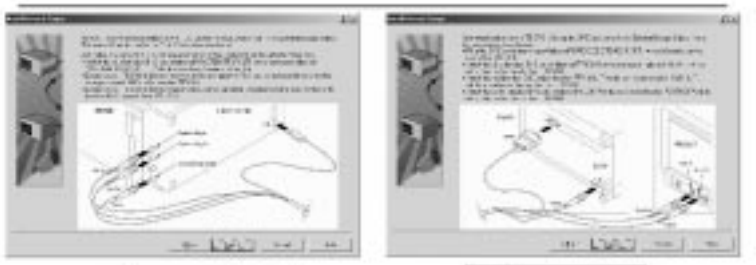


Easy Analysis with Overlay Waveforms



iView External Oscilloscope Interface

iView Setup Wizard



TLA
Connections

TDS
Connections

Integrates Seamlessly With Existing Logic Analyzer Family

- TLA600 Series: breakthrough performance at an affordable price
  - Fastest Timing in Class
  - Affordable performance
  - Open Windows® 2000
  - Analog Measurement *NEW*
- TLA700 Series: high performance logic analyzers
  - High Performance Modules
  - Flexible Mainframes
  - Analog Measurement Capability Above 1 GHz *NEW*

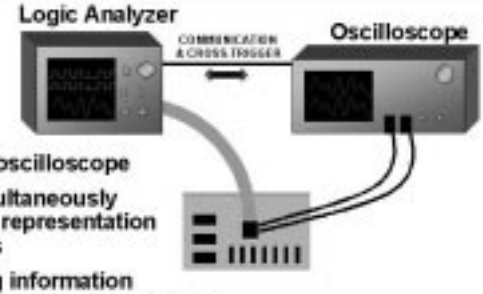
Integrates Seamlessly With Tektronix Oscilloscopes

- TDS7000 Series DPO
  - 4GHz real-time bandwith
  - 20Gs/s sample rate
  - Uses SiGe technology
  - Digital Phosphor technology
- TDS684C/694C
  - 3-GHz real-time bandwidth
  - 10-GS/s sample rate on all 4 channels simultaneously
- TDS3000 Series DPO
  - Digital Phosphor technology
  - Display, store and analyze 3 dimensions in real-time

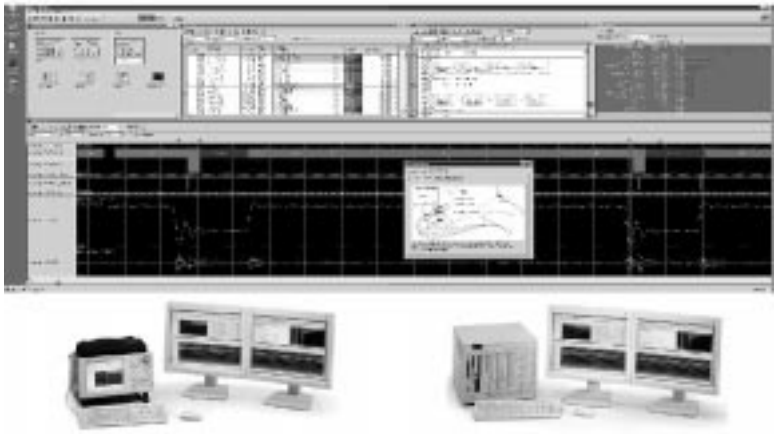
Featured on future Tektronix Oscilloscopes, too!

iView Example - DDR Memory Interface

- The Logic Analyzer traces the flow of DDR transactions
- The Logic Analyzer triggers on incorrect data and triggers the oscilloscope
- The oscilloscope simultaneously acquires a full analog representation of the relevant signals
- iView transfers analog information from the oscilloscope to the logic analyzer integrated display and automatically correlates it to the DDR bus activity
- The designer now sees how the integrity of those signal affects digital operation at the time of failure



New TLA700 Multi-Monitor Support



iView Solves Signal Integrity Challenges In Today's Digital Designs

- Integrated solution that addresses signal integrity challenges in any design
- Easy to set up when you need more visibility
- Automatic correlation
- View all data simultaneously
- Available for customers with existing instruments