Gigahertz signaling technologies: RSL, QRSL and Quad SerDes

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As electronic devices continue to get faster, the interconnect between chips becomes increasingly more important. This paper reviews the characteristics of three viable signaling solutions: RSL, QRSL and Quad SerDes - all of which are capable of transferring information at over a gigabit per second.

Rambus first introduced RSL (Rambus Signaling Level) in 1992, at a 500MHz data rate. Over time this signaling has increased to 1066MHz today, with headroom to increase in the future. In 2000, Rambus introduced its next generation signaling technology, QRSL (Quad Rambus Signaling Levels), offering twice the data rate per pin or in excess of 2Gb/s. Rambus also introduced a high-speed serial link for point to point applications running at 3.125GHz. This paper explores the technical capabilities of each of these signaling technologies, how they work and how to use them.

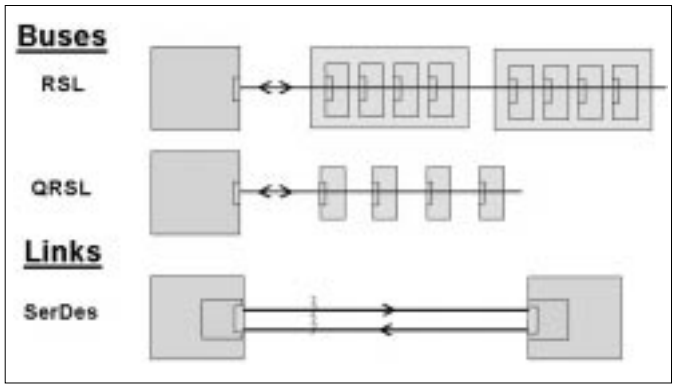

Figure 1 Rambus Bus and Link Technologies

Bus and Link Interconnects

Rambus offers three types of chip interconnection technology for bus and link topologies, as shown in Figure 1. The first is RSL introduced in 1992, first productized in 1995 and intended for multiple-connection busses, such as PC main-memory. Rambus' newest signaling, QRSL is intended for small, multiple-chip connection systems. These include small memory subsystems and chip-to-chip interconnects. The Quad SerDes interface, introduced in 2000, is a high-speed serial point-to-point interface technology designed to connect two chips together across a backplane through connectors.

Rambus Signaling Level (RSL)

RSL was Rambus' first signaling technology. Initially, RSL was introduced with data rate of 500MHz and has since been enhanced over time to over 1GHz data rate.

RSL combines many techniques, topologies and circuits resulting in the ability for a system to run at these high data rates.

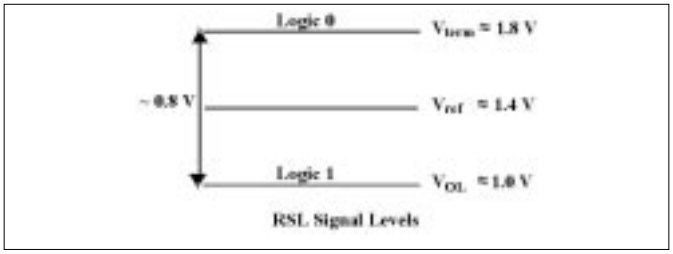

Figure 2 RSL Signal Levels

There are many factors that allow RSL to run at these speeds. One factor is the low voltage swing (800mV p-p) coupled with current mode output drivers, which adjust automatically. By using controlled impedance design techniques, a constant voltage swing is maintained, even if the target system impedance changes from 28 to 40 Ohms. Each output driver is capable of driving 30 mA maximum, across worst case process, voltage and temperature variations. Packages have low parasitic capacitance, and care is taken in the design to minimize crosstalk and inductance. A typical RDRAM package is shown in Figure 3.

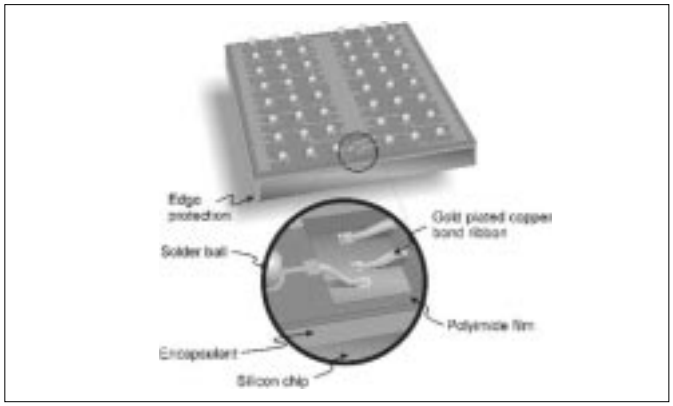

Figure 3 uBGA RDRAM Package

RSL is also the first signaling used on DRAMs to transfer data on both edges of clock, along a bidirectional bus that is multiple clock cycles long electrically. This means that at any one time, several bits of information may be in flight from the controller to the DRAMS (commands) as well as from the DRAMs back to the controller (data). All of the signal pins, including clock travel the same distance and thus take the same amount of time to travel, keeping skew between pins and between clock, data and commands at an absolute minimum.

The drivers and receiver circuits on chip are highly advanced. The input receivers are pseudo-differential, with a single common Vref pin for all input signals. On chip DLLs assure that data is sampled squarely on both the rising and falling edge of clock and that transmitted data is sent in 90 degrees out of phase to the clock. Clock itself is a differential clock, allowing a precise point of reference. Every device on the channel actually contains two clock-pairs as inputs. One of the clocks is used for transmit and the other for receive. A simple loop starting at the end of the RDRAM array travels toward the controller actually enters the controller and goes back through the RDRAM array to the end of the channel, where it is terminated along with all the other RSL signals which start at the controller. The clock loop is shown in Figure 4. The controller end of an RSL channel is unterminated.

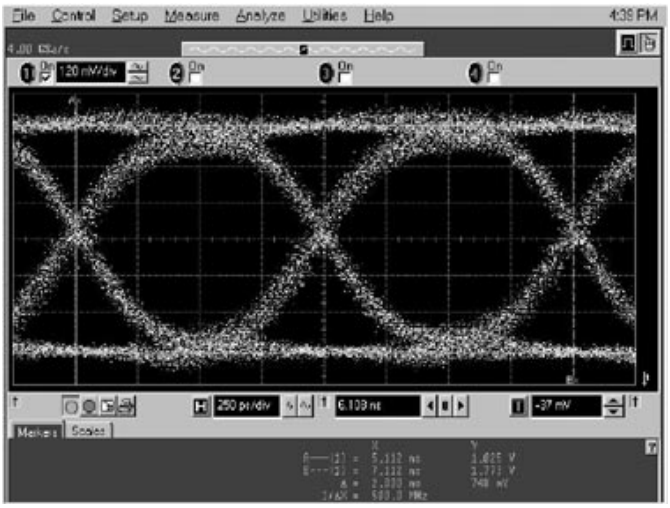

Figure 5 1GHz RSL Eye Diagram

The combination of all these techniques results in a signaling technology that transfers data at over 1GHz with headroom to support higher frequencies in the future. The eye diagram shown in Figure 5 demonstrates high quality signaling.

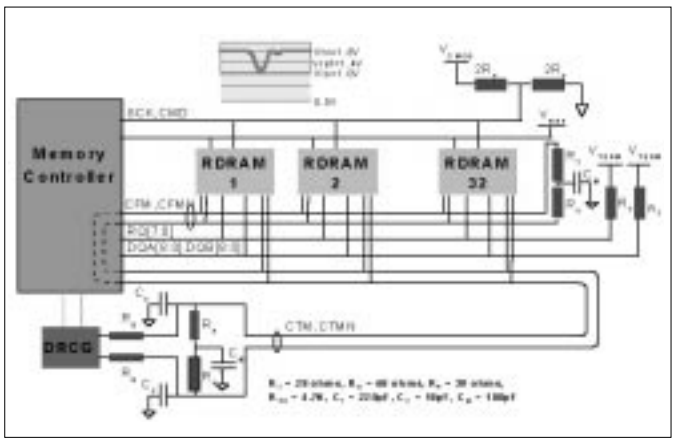

Figure 4 Rambus Channel Schematic

Quad Rambus Signaling Levels (QRSL)

QRSL signaling technology is fundamentally different from RSL. Almost all chip interconnect technology today transfers data using binary information, representing 0's and 1's with two voltage levels. QRSL doubles the data rate by using four voltages to represent two bits of information. This multi-level signaling allows higher data bandwidth, twice that of RSL (>2Gb/s) while not increasing the frequency of operation of the Channel.

Figure 6 shows an eye diagram of a QRSL driver.

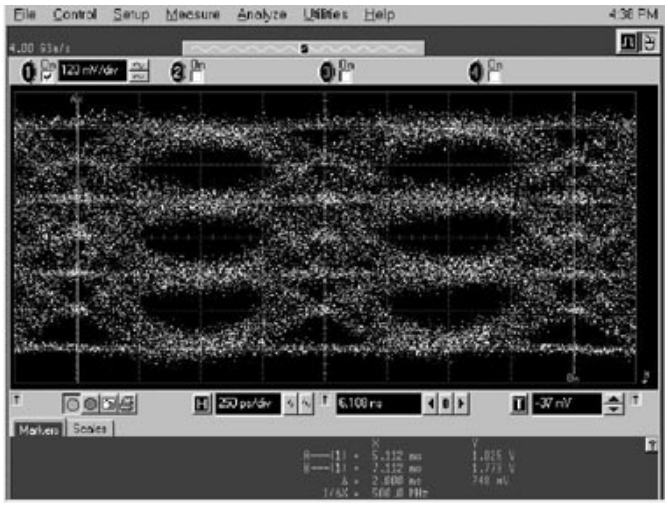

Figure 6 2Gb/s QRSL Eye Diagram

Like RSL, QRSL is a small swing signal (800 mV p-p max) and four levels each about 267 mV apart, as shown in Figure 7. Automatic current control circuitry constantly adjusts the current for voltage and temperature changes - assuring proper operation from chip to chip regardless of process variations. Since current is adjusted, the actual impedance of the system can vary to suit specific system requirements or variations in manufacturing but would typically be targeted to about 40 Ohms.

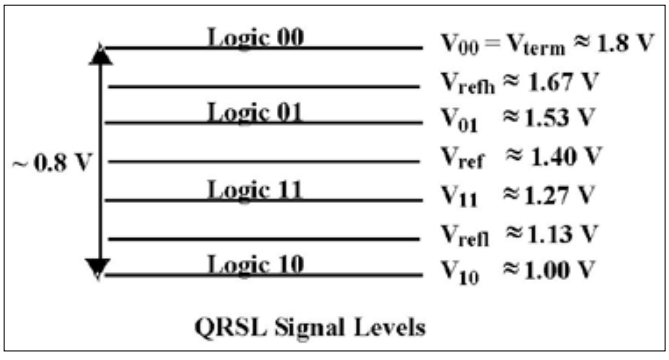

Figure 7 QRSL Signaling Levels

Common to all high-speed signaling technologies is the use of low parasitic packages, and like RSL, QRSL transfers data on both edges of the clock. The difference, of course, is that two bits of information encoded on four voltages levels are transferred per clock edge. These levels are gray coded so that keeping the LSB equal to zero allows changes in the MSB to cause a full swing signal, which is backwards compatible with RSL.

Like RSL channels, a QRSL channel is both multi-drop and bi-directional.

The input receivers and output drivers of a QRSL device are optimized for multilevel signaling. Each channel pin has a pseudo-differential integrating receiver and uses all three reference voltages. The output drivers are capable of generating three different voltage levels, and constantly adjust to keep the voltages constant even during power and temperature variations.

The channel for QRSL is much the same as RSL, except limited to about four slaves (DRAMs). The channel is terminated at the far end of the channel, away from the controller.

Quad Serializer/Deserializer (SerDes)

In April 2000, Rambus disclosed a new signaling technology primarily intended for chip-to-chip and long (~30 inches) backplane interconnect. The first implementation runs at 3.125Gb/s.

Although many of the same circuit and system design techniques are used to design the SerDes, it is very different from both the RSL and QRSL signaling.

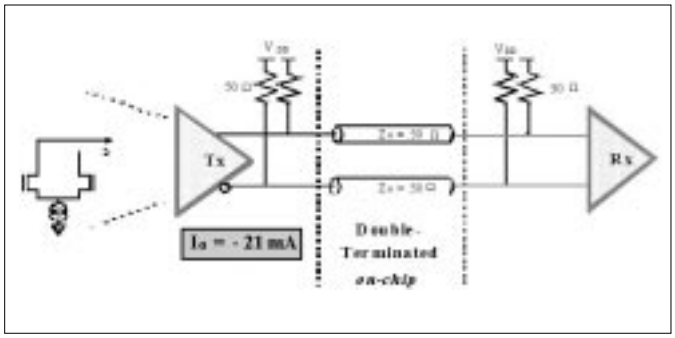

Figure 8 SerDes Link Interconnect

As is shown in Figure 8, each SerDes signal consists of a pair of differential pins. There are separate transmit and receive pins. A low-voltage swing of about 500mV is typical, as is shown in Figure 9.

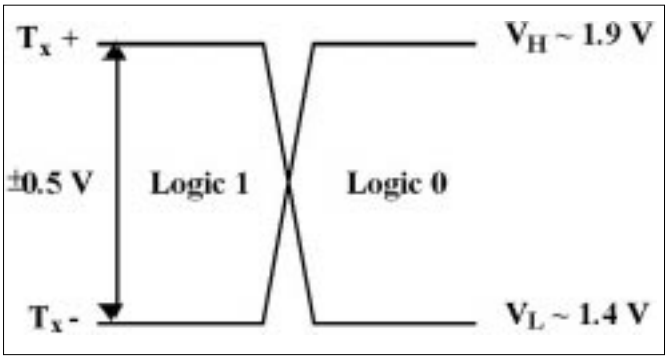

Figure 9 SerDes Signal Levels

The output drivers are current mode, both adjustable and programmable. Output current is set via an external reference resistor. Typically most systems target an impedance of about 50 Ohms, using 20mA drivers.

Data can be encoded on the output using an 8b/10b code that transmits 10bits for every 8 bits of information clocked in. This guarantees a transition edge, and limits the lower frequency spectrum of the interconnect.

These differential pair signals are unidirectional and point-to-point only - they are not configurable in a bussed system.

Depending on interconnect distance, many bits of information can be in flight along the interconnect.

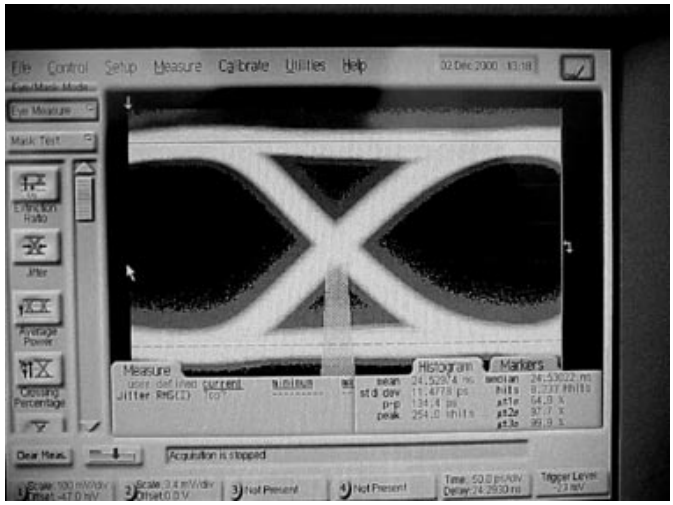

Figure 10 SerDes Low Signal Jitter

Although the driver and receiver are typically on different chips and the frequency of both is approximately the same, the SerDes cell is capable of recovering information from a transmitting cell, even if the clock source is not the same. Provided that the clocks are within a standard error of 100ppm, the receiver will be able to recover the information. An example of the low jitter characteristics of the SerDes cell is shown in Figure 10.

Comparison of RSL, QRSL and SerDes

QRSL uses the same frequency clock as RSL, but transfers twice as may bits per clock edge by further subdividing the voltage swing into four levels. Figure 11 shows the same bit pattern being transmitted in RSL and twice in QRSL.

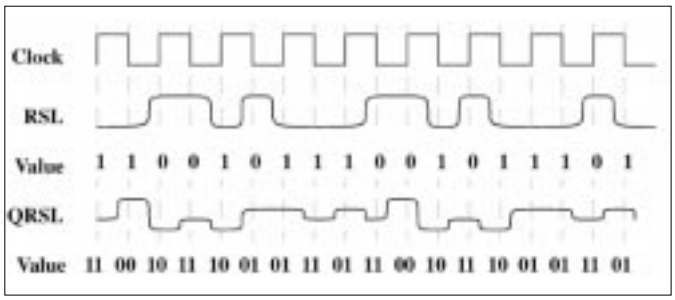

Figure 11 RSL and QRSL Signaling

The following table lists the major differences between the three signaling technologies.

Table 1 Signaling Technology Differences

	RSL	QRSL	Quad SerDes
Application Areas	Main-Memory	Small Memories, Chip-to-Chip	Chip-to-Chip across backplanes
Type	Multi-drop, Bidirectional Bus	Multi-drop, Bidirectional Bus	Point-to-Point, unidirectional link
Data Rate per link	800MHz	1.6Gb/s	3.125Gb/s[1] (4 links)
Number of Devices	32 slaves	4 slaves	2 devices
Length of Interconnect	~ 20 in.	~ 4 in.	~ 30 in.
Connectors	Yes	Not initially	Backplane connectors
Voltage Swing	800 mV	800 mV	±500 mV differential[2]
Voltage Levels	2	4	2
Clock Frequency	400MHz	400MHz	Embedded Clock
Separate Clocks	Yes	Yes	No

Table 1 Signaling Technology Differences

Future Signaling Roadmap

As RSL has evolved over time, and has increased in frequency, future enhancements to all three signaling technologies will continue to push bandwidth/pin higher to meet the ever increasing demands found in future consumer, communications and PC systems.

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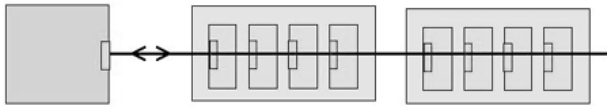
[1] *SerDes uses a differential pair of pins per connection, and the data is encoded as 10 bits for every 8 bits transmitted, yielding 2.5Gb/s per pair of pins.*

[2] *Two outputs switch at 500mV each, yielding a 1V input differential input to the receiver, ignoring loss.*

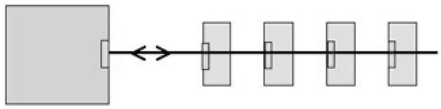
Rambus Signaling Solutions

Buses

RSL



QRSL



Links

SerDes

- Two Basic Types: Bus and Link

Rambus Signaling Solutions

- RSL 800 MHz - 1.2GHz
  - Multidrop, bi-directional with connectors
  - Good fit for small systems to large main-memory subsystems
- QRSL - Twice RSL - 1.6 to 2 Gb/s/pin
  - Backwards compatible with RSL
  - Multidrop, bi-directional - small systems, few loads
- SerDes 3.125 GHz
  - Differential, point-to-point, unidirectional
  - Designed with long interconnect, backplanes in mind

Continuing to improve signaling solutions

Rambus Signal Level
RSL