APPLICATION NOTE

- TDA8764ATS -
10-BIT A/D CONVERTER
DEMONSTRATION BOARD

AN/99042

Philips
Semiconductors

PHILIPS

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DEMONSTRATION BOARD

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CONTENTS

1. MAIN FEATURES OF THE TDA8764ATS/TDA8764AHL: 5

2. PRINCIPLE AND DESCRIPTION OF THE BOARD: 6

3. OVERVIEW OF THE BOARD: 8

4. PCB DESIGN: 10

4.1 MICROSTRIP LINES: 11
4.2 POWER SUPPLY WIRE: 11
4.3 ANALOG AND DIGITAL RETURN GROUND POINT: 11

5. SPECIAL FEATURES OF THE APPLICATION BOARD: 12

5.1 ADC ANALOG INPUT VI: 13
5.2 DATA OUTPUT D0 TO D9: 15
5.3 DATA RANGE OUTPUT IR: 18
5.4 ADC ANALOG, DIGITAL AND OUTPUT STAGES POWER SUPPLIES: 18
5.5 REFERENCE VOLTAGES VRB AND VRT: 18

6. ENVIRONMENT CIRCUITS: 19

6.1 GENERAL POWER SUPPLY: 19
6.2 TOP REFERENCE VOLATGE REGULATOR: 21
6.3 BOTTOM REFERENCE VOLTAGE: 22
6.4 CLOCK JITTER: 23
6.5 CLOCK OSCILLATOR: 25
6.6 CLOCK INTERNAL/EXTERNAL SELECTOR: 26
6.7 D FLIP-FLOP INTERFACE: 27

7. OPERATING MODE: 28

7.1 INTERNAL CLOCK OPERATION: 28
7.2 EXTERNAL SINGLE CLOCK OPERATION: 28
7.3 QUICKVIEW OF THE DEMOBOARD: 29

8. PERFORMANCES: 30

8.1 DEFINITION OF THE MEASURING PARAMETERS: 30
8.2 MEASUREMENT OF THE 60MSPS WITH BINARY OUTPUTS: 34
8.3 MEASUREMENT OF THE 60MSPS WITH BINARY OUTPUTS: 36
8.4 MEASUREMENT OF THE 60MSPS WITH CLOCK OSCILLATOR: 37

9. DEMOBOARD FILES: 39

9.1 TDA8764ATS SSOP28 VERSION: 39
9.2 COMPONENTS LIST: 39

SUMMARY

The **TDA8764** is a 10-bit high-speed **A**nalog-to-**D**igital **C**onverter designed for video data digitizing, radar pulse analysis, medical imaging and other applications. It converts the analog input signal into 10 bits binary, into two's complement or into gray digital words at a maximum sampling rate of 60Msps.

The reference voltage of the quantization ladder is external with the **TDA8764ATS** and **TDA8764AHL** versions.

Eight versions of this device exist:

TDA8764ATS/4

- **4**: 40 Msps.
  6: 60
- **TS**: SSOP28 package.
  HL: LQFP32
- **A**: with external reference voltage of the quantization ladder

This **A**pplication **N**ote describes the design and the realization of the **Demonstration Board** using the **TDA8764ATS** version (n° 709) with an application environment.

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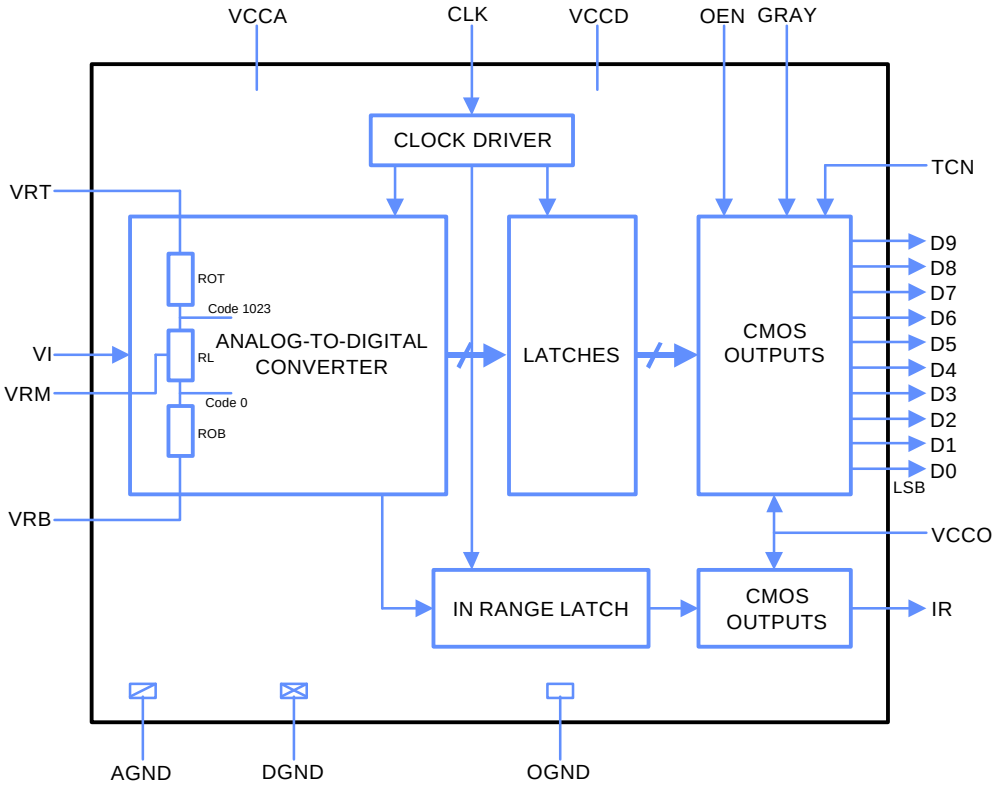
1. MAIN FEATURES OF THE TDA8764ATS/TDA8764AHL:

The **TDA8764ATS/TDA8764AHL** is a 10-bit **A**nalog-to-**D**igital **C**onverter. It can convert a typical analog input signal into 10 bits binary digital words at a maximum sampling rate of 40 **M**ega **s**ample **p**er **s**econd with a typical power dissipation of 210mW for the **TDA8764ATS/4/TDA8764AHL/4,** and at a maximum sampling rate of 60 Msps with a typical power dissipation of 310mW for the **TDA8764ATS/6/TDA8764AHL/6**. The **TDA8764ATS/TDA8764AHL** codes the binary, the two's complement or the gray digital words with 3.3V CMOS digital outputs. The block diagram and the main specifications points of this device are shown on **Figure 1**.

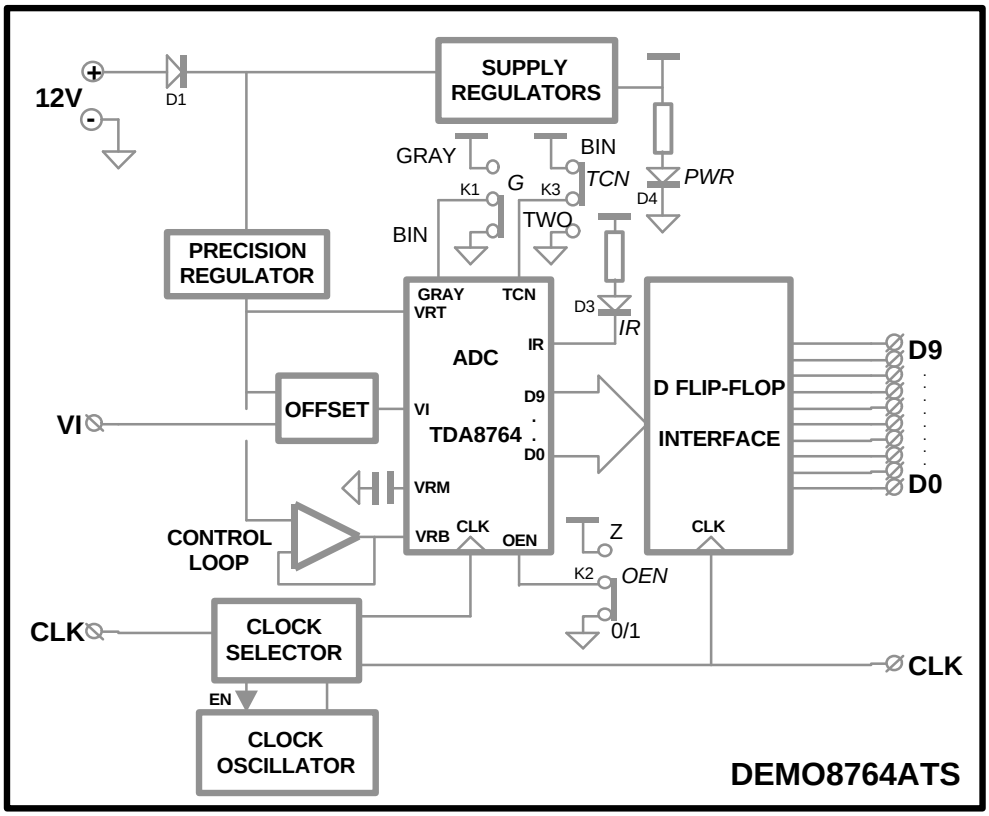
- Clock frequency: 40 or 60Msps
- Output voltage: 3.3V.
- Power dissipation (typical): 210mW (40Msps version), 310mW(60Msps version).
- Accuracy: 10-bit.
- Supply: 5V with output stages at 3.3V.
- Compatibility: input: TTL and CMOS, output: TTL, CMOS (3.3V).



- Figure 1. TDA8764ATS/TDA8764AHL block diagram -

2. PRINCIPLE AND DESCRIPTION OF THE BOARD:

The principle of the **Demo**nstration **Board** for the **TDA8764ATS**, which is described in this **A**pplication **N**ote, is shown on **Figure 2**.



- Figure 2. Functional block diagram of Demoboard -

The different blocks of the **Demoboard** are:

- A power **supply regulator** used to supply all the circuitry on the board.
- A voltage **precision regulator** supplying the ADC reference voltage TOP input V_{RT} and polarizing the control loop and the input bridge offset.

- A voltage **control loop** circuit making the ADC reference voltage BOTTOM input V_{RB} of the quantization ladder, allowing to compensate the different thermal variations of the voltage values.

- A control **offset** bridge polarising the ADC analog voltage input **VI**.

- A **D flip-flop interface** synchronising the ADC data output.

- A **clock oscillator** producing an internal clock on the **Demoboard**.

- A **clock selector** selecting the internal clock or the external clock automatically on the **Demoboard** for the ADC and the latch interface.

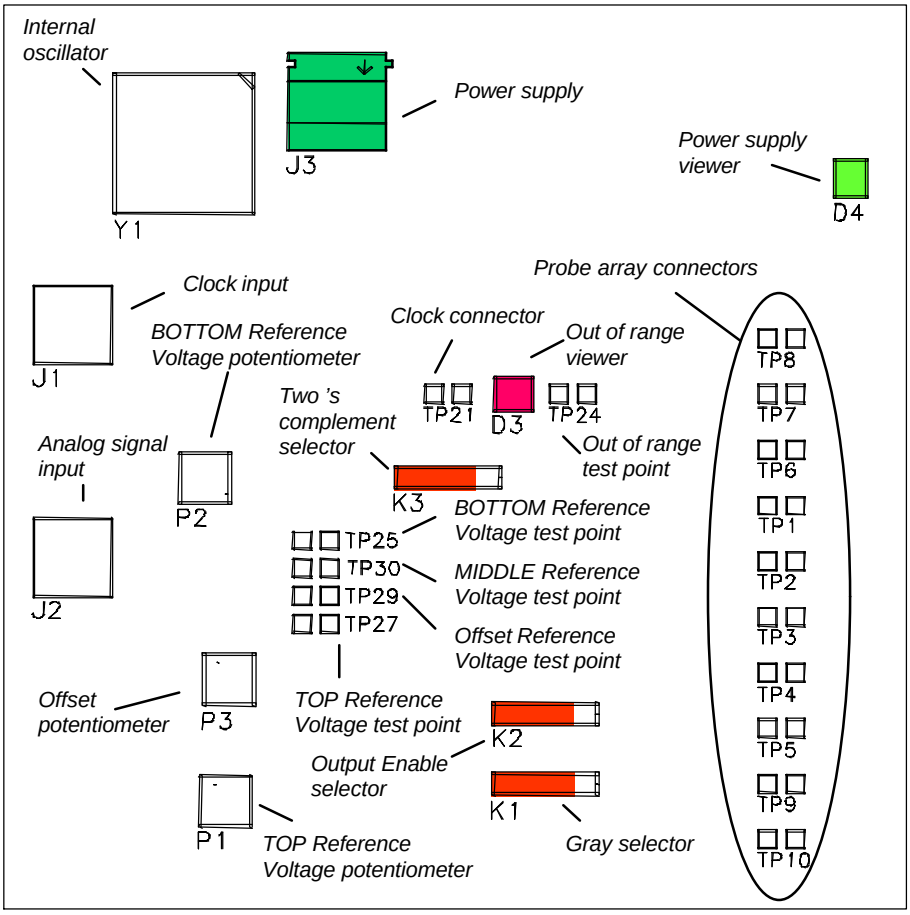
The **Demoboard** works with a single $+12V_{DC}$ external power supply. All circuitry is protected from reverse polarity. The good supply plugging is indicated by the green LED.

The overflow and the underflow of the input analog signal **VI** is indicated by the red LED.

The sample clock signal on the **Demoboard** can be internal or external by plugging the square generator in the **CLK** SMA connector. In this case the output impedance of this generator must be 50Ω.

3. OVERVIEW OF THE BOARD:

The whole implantation of the **TDA8764ATS Demoboard** version is shown on **Figure 3**.



- Figure 3. Overview of Demoboard -

The different connectors, potentiometers, switches, lights and test-points available on the board are:

- **For the general power supply:**

1. A two-points PHOENIX connector **J3** for **12V$_{DC}$** and **GND**.
2. A **PWR** green light **D4** to indicate the good supply plugging.

- **For the DC voltage adjustment values:**

1. Three chip potentiometers **P1**, **P2** and **P3** to adjust respectively the **V$_{RT}$** TOP reference voltage, the **V$_{RB}$** BOTTOM reference voltage and the **V$_{OFS}$** analog input offset of the ADC.
2. Four test-points **TP27**, **TP25**, **TP30** and **TP29** to control respectively the **V$_{RT}$**, **V$_{RB}$** and **V$_{RM}$** reference voltages and **VI+V$_{OFS}$** values.

- **For the evaluation of the TDA8764ATS:**

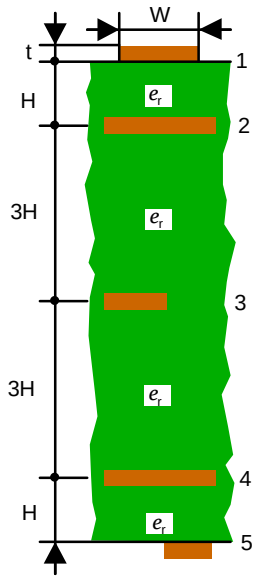
1. A SMA **J2** connector with 50Ω for the analog input signal **VI**.
2. A SMA **J1** connector with 50Ω for the external clock input **CLK**.
3. A switch **K2** to enable the ADC outputs by the input **OEN**.
4. A switch **K3** to choose the ADC two's complement outputs by the input **TC**.
5. A switch **K1** to choose the ADC gray outputs by the input **GRAY**.
6. A **IR** red light **D3** associated with the **TP24** indicating the out of range of the input analog signal.

- **For the reconstruction of the analog input waveform:**

1. Ten-probe array connectors **TP1** to **TP10** corresponding to the ADC digital output **D0** to **D9** are available to connect the logic analyser which computes the data.
2. A connector **TP21** corresponding to the ADC clock.

4. PCB DESIGN:

The design is made on a multilayer **P**rinted **C**ircuit **B**oard. The technological concept used to make this PCB is given on **Figure 4**.



- Figure 4. PCB structure -

Five physical copper layers are used. The first and fifth layers are the signal layers which contain the microstrip lines. The second and fourth layers constitute the ground planes corresponding to the signal layers. The third layer is designed specially for the power supply wires.

The metallic hole technique is employed to make all the necessary interconnections between the layers. The dielectric substrate used is an Epoxy Glass resin with a relative permittivity ($\boldsymbol{e}_r$) of 4.7 and a copper thickness (**t**) of 35µm (≈1.4mils). The substrate thickness (**H**) is ≈0.2mm (8mils) between the copper layers.

4.1 MICROSTRIP LINES:

To calculate the width (**W**) of these 50Ω matched lines, the Kaup's relation was used:

$$W = \frac{5.98H}{0.8e^{\frac{Zo\sqrt{e_r+1.41}}{87}}} - \frac{t}{0.8},$$

(Accurate to within 5% when $0.1 < \frac{W}{H} < 3.0$ and $1 < e_r < 15$).

hence:

W = 12.71mils/≈0.32mm,

where:

Zo = 50Ω,
t = 1.4mils/≈35µm,
H = 8mils/≈0.2mm,
e_r = 4.7.

4.2 POWER SUPPLY WIRE:

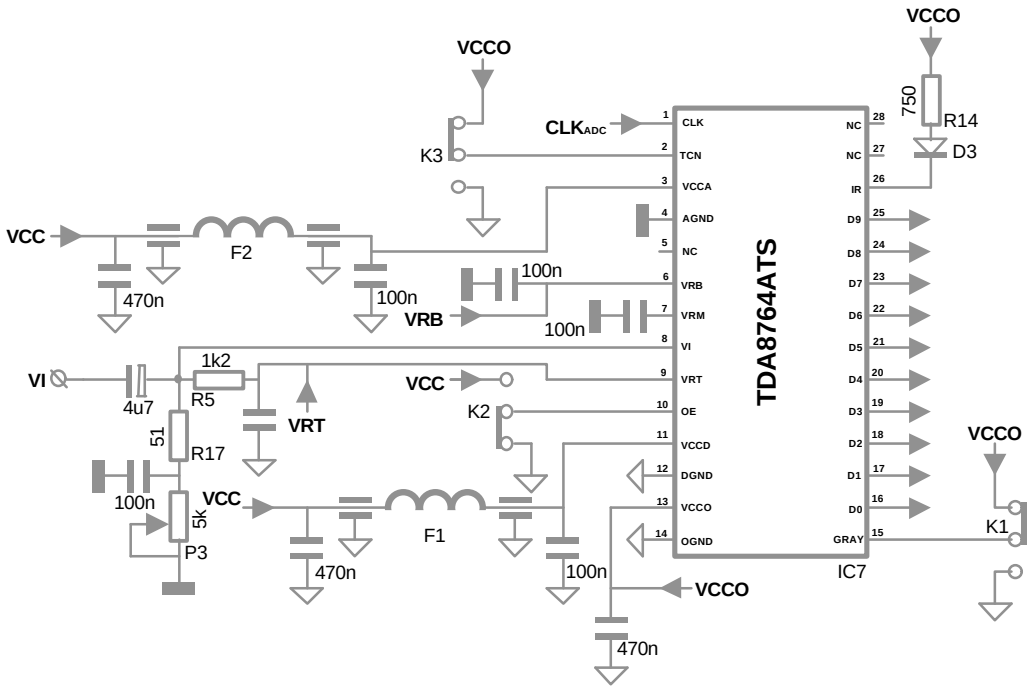
To reduce the voltage fluctuation effects due to switching currents inside the integrated circuits, the power supply wires are designed with a low characteristic impedance of microstrip lines in order to obtain a small equivalent inductance.

4.3 ANALOG AND DIGITAL RETURN GROUND POINT:

To minimise the noise due to capacitive coupling between the analog input and the digital output parts of the ADC, two separate ground planes are designed on all layers and are connected together through an inductor.

5. SPECIAL FEATURES OF THE APPLICATION BOARD:

To obtain optimal performances, the recommended application diagram is given on **Figure 5**.



- Figure 5. TDA8764ATS application diagram -

5.1 ADC ANALOG INPUT VI:

The DC offset voltage is fixed on the board by an intermediate resistor bridge made by the resistors **R12** and **R13** associated with the potentiometer **P1**. The DC offset voltage value is adjusted from the $\mathbf{V_{RT}}$ reference voltage. This reference voltage is supplied by the internal reference voltage regulator in the device.

So, the $\mathbf{V_{OFS}}$ typical offset voltage value (which corresponds to code 511/512) is obtained approximately from the relation:

$$\mathbf{V_{OFS}} = \frac{\mathbf{V_{RT} + V_{RB} - V_{OST} + V_{OSB}}}{\mathbf{2}},$$

where:

V_{RT} = 3.7V,
V_{RB} = 1.3V,
V_{OST} = 0.166V,
V_{OSB} = 0.182V.

Hence, the typical DC offset level $\mathbf{V_{OFS}}$ corresponding to code 511/512 is:

$$\mathbf{V_{OFS} = 2.508V}.$$

To ensure a sufficient analog input stability, the offset resistor bridge current I_{VI} is fixed at 1mA. The value of **P1** is obtained by:

$$R17 + P3 = R5.\left(\frac{V_{OFS}}{V_{RT} - V_{OFS}}\right) \text{ and } R5 = \frac{V_{RT} - V_{OFS}}{I_{VI}},$$

where:

R17 = 50Ω.

The dynamic analog input is connected through a 220nF AC coupling to the external generator through a 50Ω microstrip line and a **R17** = 50Ω resistor ending.

A high frequency decoupling of 100nF is added to the potentiometer **P3** so that the decoupling allows to get a good dynamic ground.

The typical peak-to-peak magnitude nominal value $VI_{p.-p}$ of the dynamic input signal is determined from the relation:

$$VI_{p.-p} = V_{RT} - V_{RB} - V_{OST} - V_{OSB} \ ,$$

hence,

$$\mathbf{VI_{p.-p} = 2.052V}.$$

The quantum of the **TDA8764ATS** is:

$$q = \frac{VI_{p.-p}}{2^{10} - 1} \ ,$$

hence,

$$\mathbf{q \approx 2mV}.$$

5.2 DATA OUTPUT D0 TO D9:

All data outputs of the **TDA8764A** are CMOS compatible and they are directly addressed to a latch interface circuit.

The switch **K3** corresponding to the two's complement input **TCN** allows the choice either the **BIN**ary or the ***TWO**'s complement* digital words which correspondence is given on **Table 1** (in fact, *the two's complement* digital words correspond to the binary digital words with the inverted MSB **D9**).

STEP	**IR**	**BINARY OUTPUT BITS**										***TWO'S COMPLEMENT* OUTPUT BITS**									
		D9	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
U/F	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
511	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
512	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
513	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1022	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
1023	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
O/F	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1

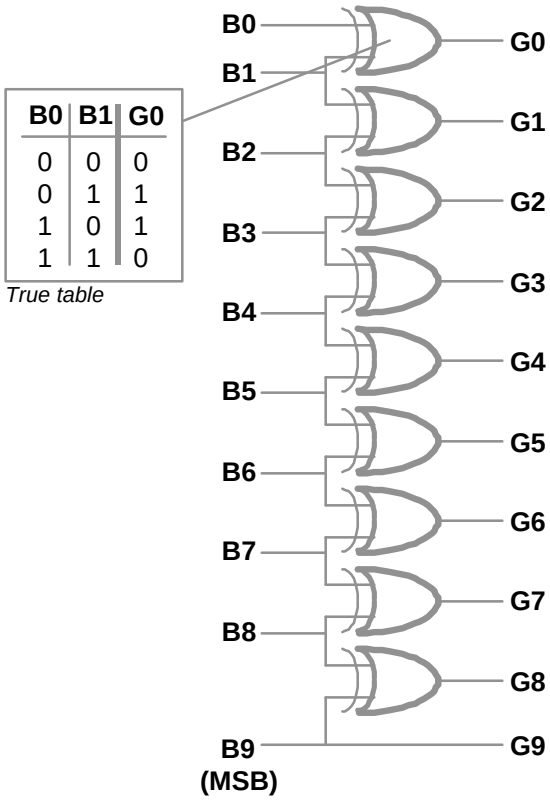
- Table 1: Binary/Two's complement output coding -

The switch **K1** corresponding to the gray input **GRAY** allows the choice either the **BIN**ary or the **GRAY** digital words which correspondence is given on **Table 2**.

STEP	IR	BINARY OUTPUT BITS										GRAY OUTPUT BITS									
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
U/F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
511	1	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
512	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
513	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1022	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1
1023	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
O/F	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

- Table 2: Binary/Gray output coding -

To find the others gray output codes, a diagram of a binary to gray function is given on **Figure 6**.



- Figure 6. Binary to gray function -

The switch **K2** corresponding to the output enable input **OEN** allows either to enable **0/1** or to put high impedance **Z** state on the data outputs.

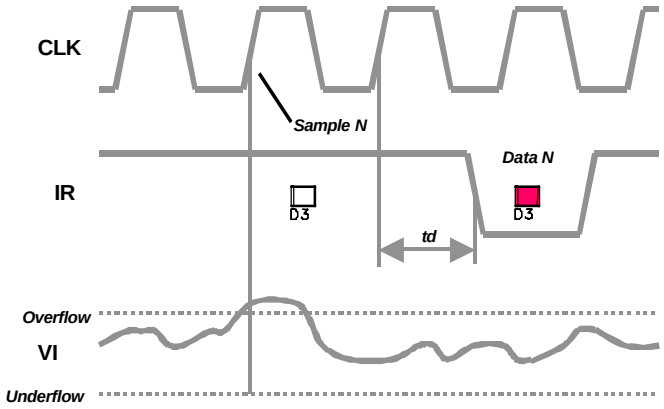
On the **Table 3** is given the correspondence between the different choices.

TCN	G	OEN	D9 to D0	IR
X	X	1	high impedance	
1	0	0	binary	active
1	1	0	gray	active
0	0	0	*two's complement*	active

- Table 3: Selection mode -

5.3 DATA RANGE OUTPUT IR:

The underflow and overflow **IR** output pin is directly connected to the red light LED **D3**. When the underflow or overflow of the **VI** analog input signal is detected, the red LED is switched on. The functional diagram is shown on **Figure 7**.



- Figure 7. IR voltage waveform -

5.4 ADC ANALOG, DIGITAL AND OUTPUT STAGES POWER SUPPLIES:

Two power supplies of 5V and 3.3V are necessary to supply the **TDA8764ATS/TDA8764AHL** respectively for the analog and digital pins and for the output stages.

To ensure a good bypassing at low and high frequencies, the use of several different parallel capacitors is required and SMD bypass π type filters are implanted on the board near the ADC on each power pins.

5.5 REFERENCE VOLTAGES VRB AND VRT:

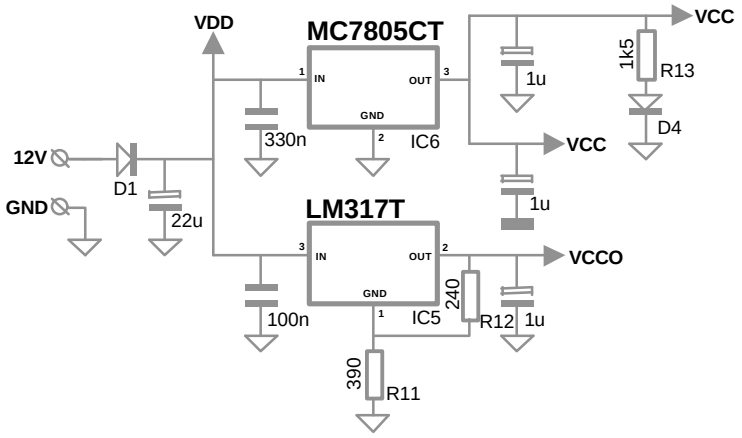
The **TOP Reference Voltage** $\mathbf{V_{RT}}$ of 3.7V is obtained from a specific IC precision voltage regulator implanted on the board. The regulator output voltage is directly applied on the $\mathbf{V_{RT}}$ pin of the ADC, a 100nF capacitor placed close to this point constitues an effective decoupling.

The **BOTTOM Reference Voltage** $\mathbf{V_{RB}}$ of 1.3V is obtainde by the control loop from a specific IC low voltage operational amplifier and a transistor. The output voltage of this control loop is directly applied on the $\mathbf{V_{RB}}$ pin of ADC.

6. ENVIRONMENT CIRCUITS:

6.1 GENERAL POWER SUPPLY:

The electrical diagram is shown on **Figure 8**. Two IC voltage regulators **IC5** and **IC6** are used directly mounted on the board and they are supplied from an external DC power unit of $12V_{DC}$/190mA. Nevertheless, the external voltage can range from $10V_{DC}$ to $15V_{DC}$.



- Figure 8. Electric diagram of the power supply -

The regulation and the stabilisation of all circuitry com from the **VDD** voltage value obtained after the protection diode **D1**. Two stabilised voltages **VCC** of 5V and **VCCO** of 3.3V are available on the **Demoboard** with the distribution:

VCC used for:	**VCCO used for:**
Internal oscillator.	D flip-flop interface.
ADC digital and analog supply voltages.	ADC output stages supply voltage.

The **VCCO** is made from a adjustable regulator IC type LM317LD from the relation:

$$VCCO = V_{ref}\left(1 + \frac{R11}{R12}\right),$$

where:

V_{ref} = 1.25V (the difference between the output and the adjustment terminal voltages),
R12 = 240Ω.

To obtain **VCCO** = 3.3V, the **R11** must be equal at:

$$R11 = R12\left(\frac{VCCO}{V_{ref}} - 1\right),$$

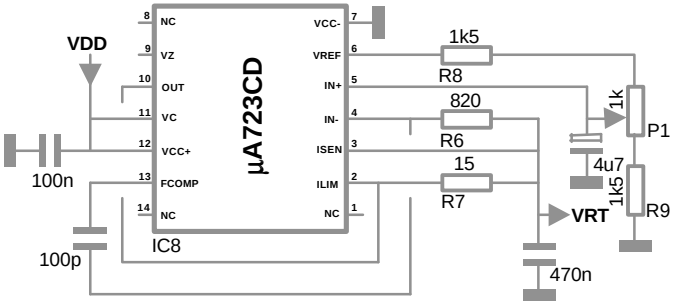
so:

R11 ≈ 390Ω.

The BYD17G Silicon diode **D1** ensures the protection of all the circuitry from reverse polarities. The good supply plugging is indicated by a green LED **D4**.

6.2 TOP REFERENCE VOLATGE REGULATOR:

The precision voltage regulator **IC8 µA723CD** of PHILIPS SEMICONDUCTORS is used and mounted as a positive low-voltage regulator. The electric diagram used is shown on **Figure 9**.

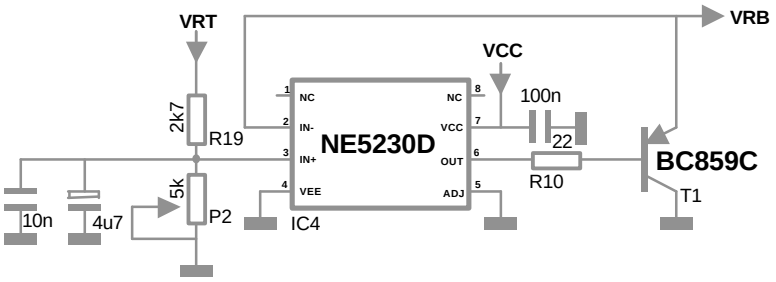


- Figure 9. Electric diagram of the TOP reference voltage -

The voltage level **VDD** obtained on the cathode of the protection diode **D1** is applied on the VCC+ (pin 12) of this device.
The nominal reference level of 3.7V is obtained from the voltage level supplied on the VREF (pin 6) of the **µA723CD**. A bridge resistor **R8** and **R9** with a potentiometer **P1** allows to adjust the reference level value on the no-inverting input IN+ (Pin 5) of the IC.
The frequency compensation of the output current amplifier stage is done with an external capacitor of 100pF connected between FCOMP (pin 13) and IN- (pin 4).

6.3 BOTTOM REFERENCE VOLTAGE:

The low voltage operational amplifier **IC4 NE5230D** associated with the transistor PNP **T1 BC859C** of PHILIPS SEMICONDUCTORS is used and mounted as a control loop stage. The electric diagram used is shown on **Figure 10**.



- Figure 10. Electric diagram of the BOTTOM reference voltage -

The $\mathbf{V_{RB}}$ voltage, controlled by the trimmer potentiometer **P2**, is connected on IN+ (pin 3) of **IC7** and is compared to IN- (pin 2) reference voltage of ADC to compensate the different thermal variations of the voltage values due to the quantization ladder.
The voltage output of the operational amplifier allows to control the conduction of the transistor **T1** which drives the current of the quantization ladder to GND. A resistor **R10** is therefore provided on the board to limit the output current in **IC7**.

6.4 CLOCK JITTER:

The jitter value of the clock signal must be low otherwise some sampling errors can appear. The jitter value can be calculated from the slope of the sinewave input signal. The sinewave input signal is given by:

$$v(t) = \frac{vi_{FS}}{2}.\sin(2.p.f_i.t),$$

where:

$vi_{FS} = 2^n.q$	: ADC full scale,
n	: ADC bit number,
f_i:	: input signal frequency.

So, the slope of the sinewave is:

$$\Delta v(t) = \Delta t.\frac{\P v(t)}{\P t} = \Delta t.\frac{vi_{FS}}{2}.2.p.f_i.\cos(2.p.f_i.t).$$

The slope is maximum at t_0=0 (middle of the input full scale):

$$\Delta v(t_0) = \Delta t_0.vi_{FS}.p.f_i,$$

hence:

$$\Delta t_0 = \frac{\Delta v(t_0)}{2^n.q.p.f_i}.$$

For a jitter below the quantum ($\Delta v(t_0)$ = q), it must be inferior at:

$\Delta \mathbf{t_0}$ **< 20ps** (**TDA87A64TS/4**),
$\Delta \mathbf{t_0}$ **< 10ps** (**TDA87A64TS/6**),

with:

n = 10,
f_i = 15MHz (**TDA87A64TS/4**),
f_i = 30MHz (**TDA87A64TS/6**).

The variation around the frequency of the sampling clock is given by:

$$\frac{\Delta f_{clk}}{f_{clk}} = \frac{\frac{\Delta t_0 . f_{clk}}{2}}{1 - \left(\frac{\Delta t_0 . f_{clk}}{2}\right)^2},$$

hence:

$$\frac{\Delta f_{clk}}{f_{clk}} \langle \pm 400\text{ppm} \quad (\textbf{TDA8764ATS/4}),$$

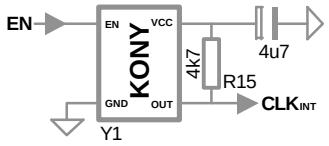
$$\frac{\Delta f_{clk}}{f_{clk}} \langle \pm 300\text{ppm} \quad (\textbf{TDA8764ATS/6}).$$

where:

f_{clk} = 40MHz (**TDA8764ATS/4**),
f_{clk} = 60MHz (**TDA8764ATS/6**).

6.5 CLOCK OSCILLATOR:

The electric diagram of the internal clock oscillator is shown on **Figure 11**. The clock oscillator uses a simple KONY tri-state oscillator integrated circuit. When the EN input is at VCC, the oscillator is enabled, otherwise it is disabled and this output is at high impedance. The **R15**=4.7KΩ resistor is implanted to fix the output level when the oscillator is at high impedance

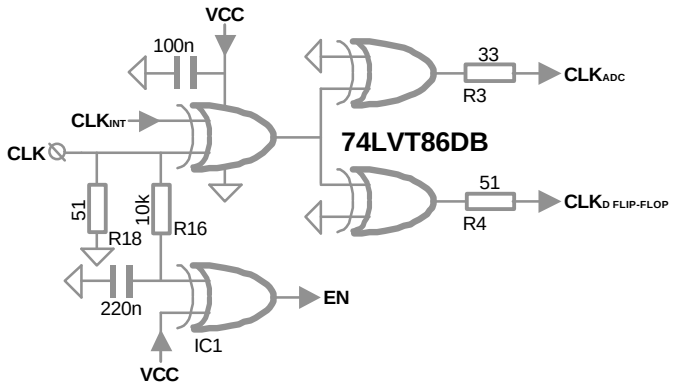


- ***Figure 11. Electric diagram of the clock oscillator –***

Depending on the ADC version implanted on the **Demoboard** (/**4** or /**6** version) the values of the oscillator **Y1** is 40MHz or 60MHz.

6.6 CLOCK INTERNAL/EXTERNAL SELECTOR:

On the **Demoboard**, a specific circuit is designed to select automatically the clock either from the oscillator on the board or from an external generator, addressing the ADC and the latch interface circuit. The electric diagram of this circuit is shown on **Figure 12** and it uses a SMD IC exclusive-or gate **74LVT86DB** from the Low Voltage Technology logic family of PHILIPS SEMICONDUCTORS.



- Figure 12. Electric diagram of the clock selector -

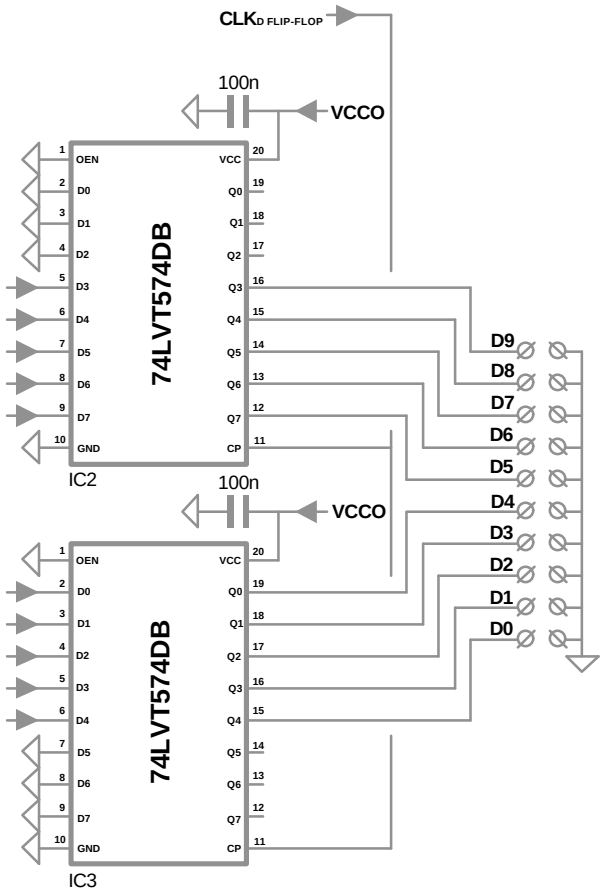
When the external CLK is used the **R16**=10KΩ resistor associated with the 220nF capacitor and the exclusive-gate disables the clock oscillator on the board. The **R3**=33Ω and **R4**=51Ω resistors are used to improve the clock signal.

Important:

In all applications, it is necessary to put a resistor (³33W), far from the ADC clock input, on the clock signal line. This resistor allows to eliminate principally the undershoot/overshoot which device does not like and to improve the clock signal.

6.7 D FLIP-FLOP INTERFACE:

The electric diagram of the D flip-flop interface is shown on **Figure 13**. It allows to recover the ADC data output synchronised on the clock sampling.



- Figure 13. Electric diagram of the D flip-flop interface -

The interface circuit uses two SMD ICs D-type flip-flop **74LVT574DB** from the Low Voltage Technology logic family.

7. OPERATING MODE:

An external power unit of 12V/190mA is required to supply the **Demoboard**. However, the board is able to work between 10V and 12V.

All DC voltage of **P1** (V_{RT}), **P2** (V_{RB}) and **P3** (V_{OFS}) are locked in the **A**pplication **L**aboratory in **PAR**is before delivery to be true to the provided product specifications.

So:

$$\mathbf{V_{RT} = 3.7V},$$

$$\mathbf{V_{RB} = 1.3V},$$

$$\mathbf{V_{OFS} = 2.508V}.$$

But the $\mathbf{V_{OFS}}$ value may be modified by the user to obtain the best full scale of the input analog signal. To do this, it's better to use the IR viewer to check if the analog input signal is out of range. In this case, the LED **D3** switches on.

Before putting the board on, please check that **K1** and **K3** are at **BIN**; and **K2** is at **0/1** (referring to the implantation diagram given on **Figure 3**).

7.1 INTERNAL CLOCK OPERATION:

The internal clock oscillator is automatically enabled when the 50Ω connector **J1** is not connected to an external clock generator.

7.2 EXTERNAL SINGLE CLOCK OPERATION:

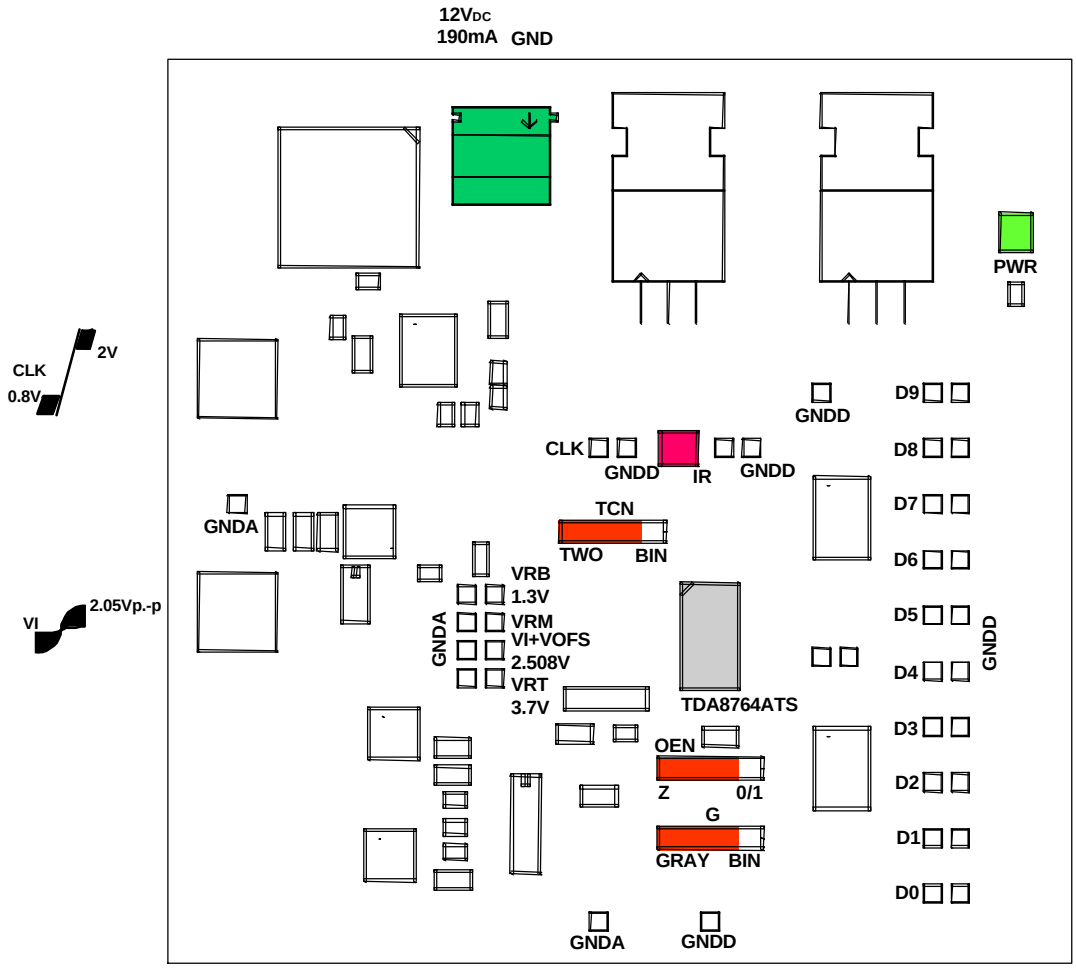
When the 50Ω is connected, by **J1** connector, to an external 50Ω square clock generator, the internal clock oscillator is automatically disabled. The required clock levels are:

$$V_{CLKH} \text{ min} = 2.0V,$$

$$V_{CLKL} \text{ max} = 0.8V.$$

7.3 QUICKVIEW OF THE DEMOBOARD:

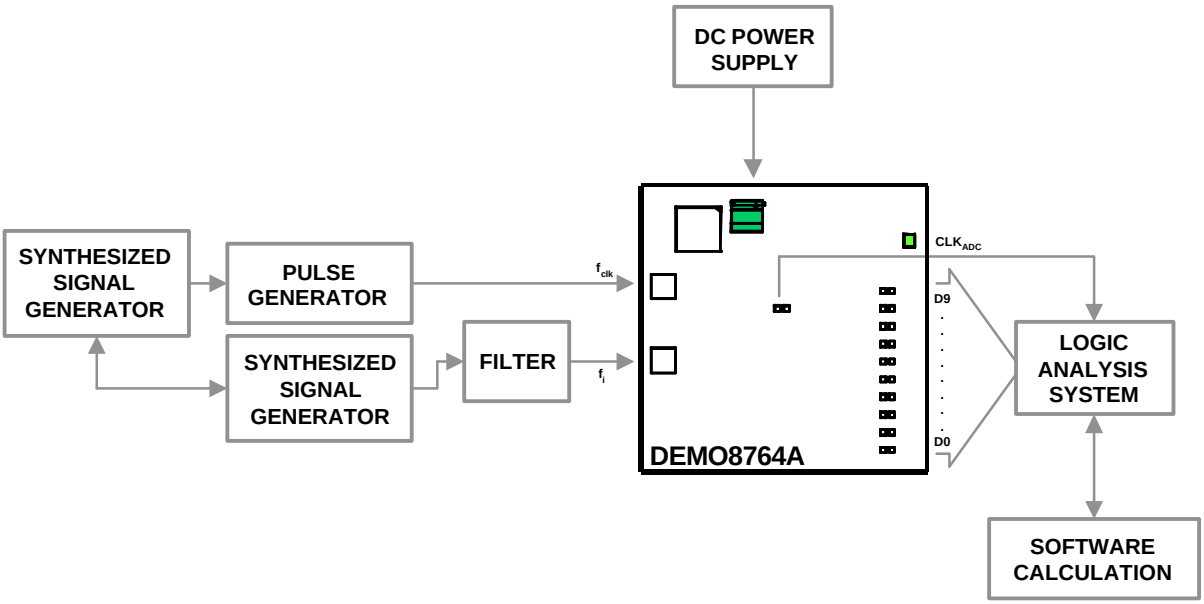
A Quick view of the **TDA8764ATS Demoboard** with main information is given on **Figure 14**.



- Figure 14. Quickview of the DEMO8764ATS -

8. PERFORMANCES:

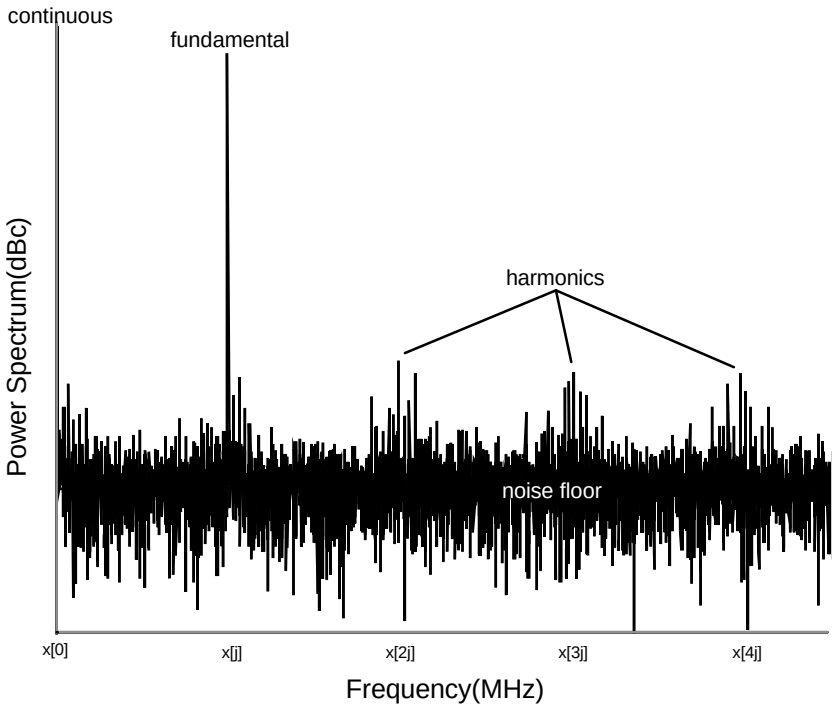
An evaluation of the **TDA8764ATS** ADC performances were made with the **Demoboard** environment on CAEN's dynamic bench which block diagram is given on **Figure 15**.



- Figure 15. CAEN's dynamic bench block diagram -

8.1 DEFINITION OF THE MEASURING PARAMETERS:

To evaluate the ADC performances on the Demoboard, the CAEN dynamic bench uses the **F**ast **F**ourier **T**ransform for dynamic parameters and the **Histogram** for *static* parameters from the sample signal.



- Figure 16. FFT -

According to the FFT shown on **Figure 16**, the main dynamic parameters are:

- The **T**otal **H**armonic **D**istortion is the ratio between the RMS signal amplitude and the RMS sum of the first five harmonics. From the power spectrum of FFT, the **THD** is calculated from the relation:

$$THD_{dBc} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2}^{6} x^2[i \times j]}}.$$

Where:

$x[j]$: fundamental component corresponding with the j spectrum component,

$x[i \times j]$: component of harmonic i.

- The **S**purious **F**ree **D**ynamic **R**ange is the ratio between the RMS signal amplitude and the RMS value of the highest spectrum component (harmonic or noise). From the FFT, the **SFDR** is calculated from the relation:

$$SFDR_{dB} = 20 \times \log_{10} \frac{x[j]}{MAX(x[i])}.$$

Where:

$x[i]$: spectrum component i with $i \in [2:\frac{N}{2}]$ (N: number of samples) and $i \neq x[j]$.

- The **SI**gnal to **N**oise **A**nd **D**istortion ratio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components. From the FFT, the **SINAD** is calculated from the relation:

$$SINAD_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2, i \neq j}^{\frac{N}{2}} x[i]}}.$$

- The **S**ignal to **N**oise **R**atio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components without harmonic used in the **THD** relation. From the FFT, the **SNR** is calculated from the relation:

$$SNR_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2, i \neq j \times [1:6]}^{\frac{N}{2}} x[i]}}.$$

- The **E**ffective number of bit is calculated by the relation (valid to NYQUIST condition):

$$E_{BIT} = \frac{SINAD - 10 \times \log_{10} \frac{3}{2}}{20 \times \log 2}.$$

The main *static* parameters are:

- The **D**ifferential **N**on**L**inearity is the difference between the measured width and the ideal width that is 1 LSB of a code i. Only the maximum and the minimum value is given.

- The **I**ntegral **N**on**L**inearity is the difference between the measure of the transition and of the ideal transition size of two consecutive codes. Only the maximum and the minimum value is given. The INL is calculated from the DNL following the relation:

$$\mathrm{INL}[i] = \sum_{j=0}^{i} \mathrm{DNL}[j],$$

where:

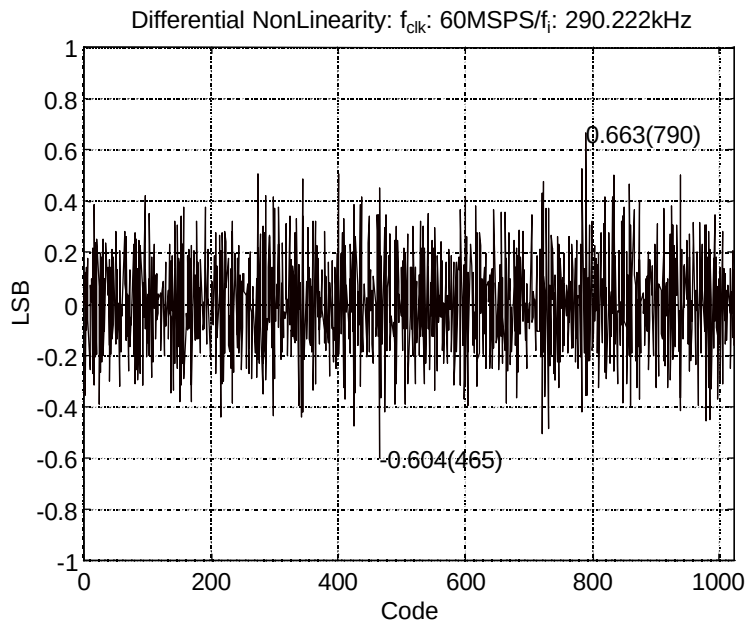
$i \in [0:2^N - 1]$ (N: number of bit).

8.2 MEASUREMENT OF THE 60MSPS WITH BINARY OUTPUTS:

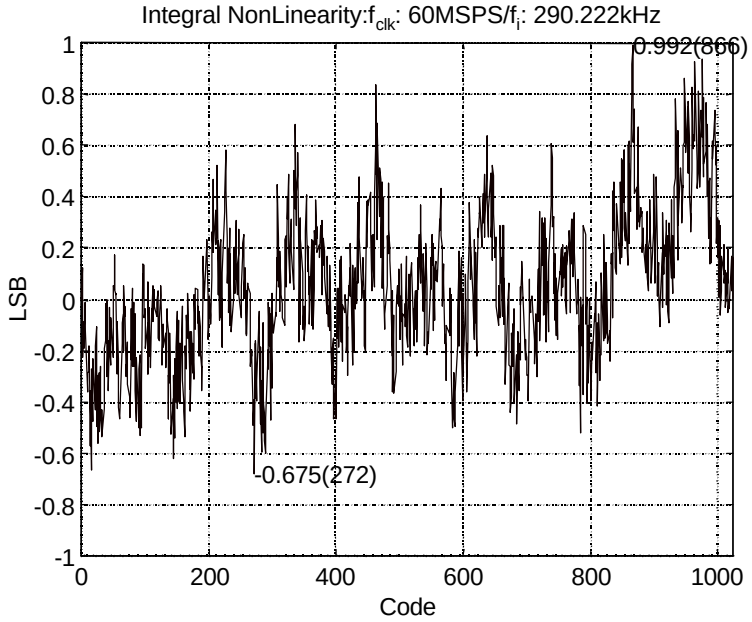
This version of the **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	300kHz.
Waveform:	Sinewave.
Magnitude:	Full Scale (FFT), Full scale +5% (DNL/INL).
Antialiasing Filter:	Yes
Clock frequency:	60Msps.
Operating mode:	External clock.
Output format:	Binary.

The typical results and the corresponding diagrams obtained with these conditions are given on **Figures 17 and 18**.



- Figure 17. DNL result of 60Msps in binary mode -



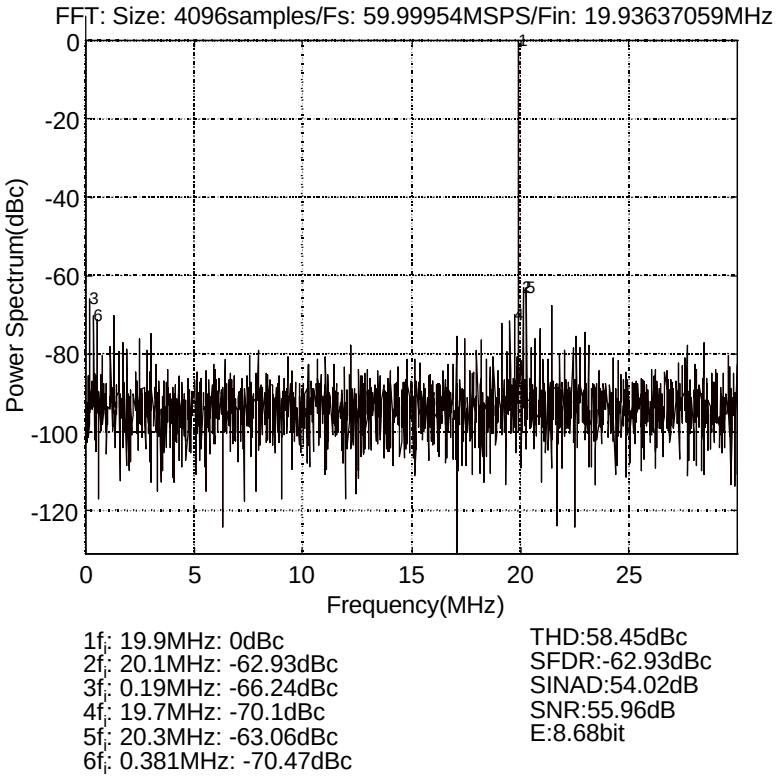
- Figure 18. INL result of 60Msps in binary mode -

8.3 MEASUREMENT OF THE 60MSPS WITH BINARY OUTPUTS:

This version of the **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	20MHz.
Waveform:	Sinewave.
Magnitude:	Full Scale.
Antialiasing Filter:	Yes
Clock frequency:	60Msps.
Operating mode:	External clock.
Output format:	Binary.

The typical results and the corresponding diagrams obtained with these conditions are given on **Figure 19**.



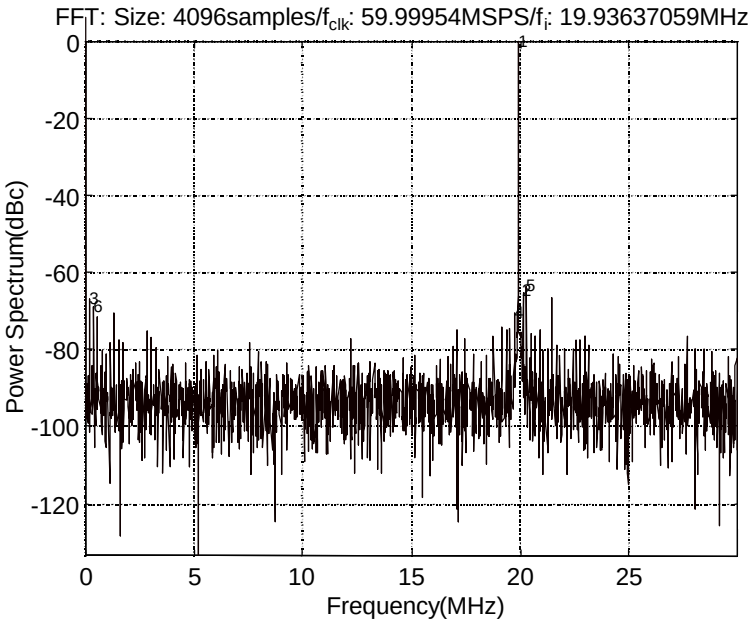
- Figure 19. FFT results of the 60Msps in binary mode -

8.4 MEASUREMENT OF THE 60MSPS WITH CLOCK OSCILLATOR:

The **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	20MHz.
Waveform:	Sinewave.
Magnitude:	Full Scale.
Antialiasing Filter:	Yes
Clock frequency:	60Msps.
Operating mode:	Internal clock.
Output format:	Binary/Gray/*Two's complement*.

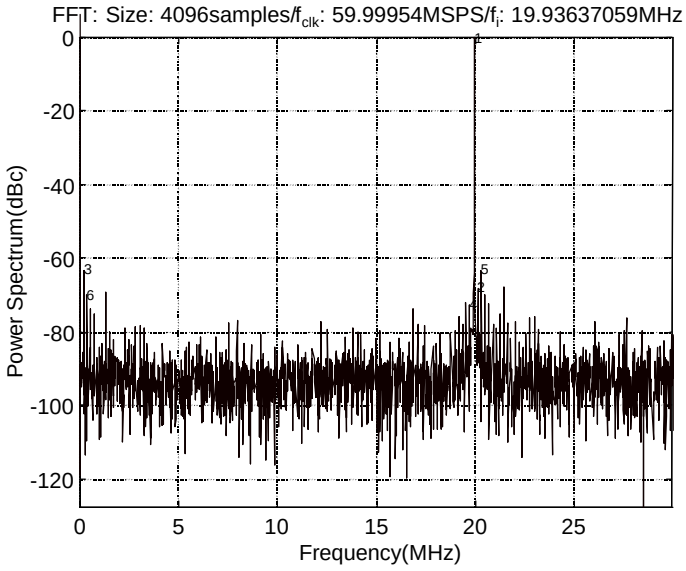
The typical results and the corresponding diagrams obtained with these conditions are given from **Figure 20 to 22**.



$1f_i$: 19.9MHz: 0dBc
$2f_i$: 20.1MHz: -64.98dBc
$3f_i$: 0.19MHz: -66.8dBc
$4f_i$: 19.7MHz: -70.45dBc
$5f_i$: 20.3MHz: -63.35dBc
$6f_i$: 0.381MHz: -69.09dBc

THD:59.2dBc
SFDR:-63.35dBc
SINAD:53.32dB
SNR:54.62dB
E:8.56bit

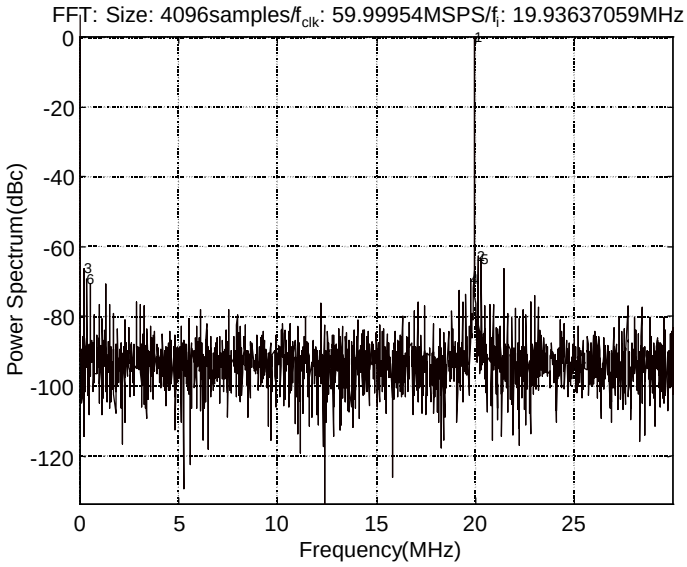
- Figure 20. FFT results of the 60Msps with clock oscillator of Demoboard in binary mode -



$1f_i$: 19.9MHz: 0dBc
$2f_i$: 20.1MHz: -67.97dBc
$3f_i$: 0.19MHz: -63.1dBc
$4f_i$: 19.7MHz: -72.44dBc
$5f_i$: 20.3MHz: -63.28dBc
$6f_i$: 0.381MHz: -69.92dBc

THD:58.93dBc
SFDR:-63.1dBc
SINAD:52.8dB
SNR:54.01dB
E:8.48bit

- Figure 21. FFT results of the 60Msps with clock oscillator in Gray mode -



$1f_i$: 19.9MHz: 0dBc
$2f_i$: 20.1MHz: -62.71dBc
$3f_i$: 0.19MHz: -66.12dBc
$4f_i$: 19.7MHz: -69.5dBc
$5f_i$: 20.3MHz: -63.61dBc
$6f_i$: 0.381MHz: -69.24dBc

THD:58.4dBc
SFDR:-62.71dBc
SINAD:53.11dB
SNR:54.64dB
E:8.53bit

- Figure 22. FFT results of the 60Msps with clock oscillator in Two's complement mode -

9. DEMOBOARD FILES:

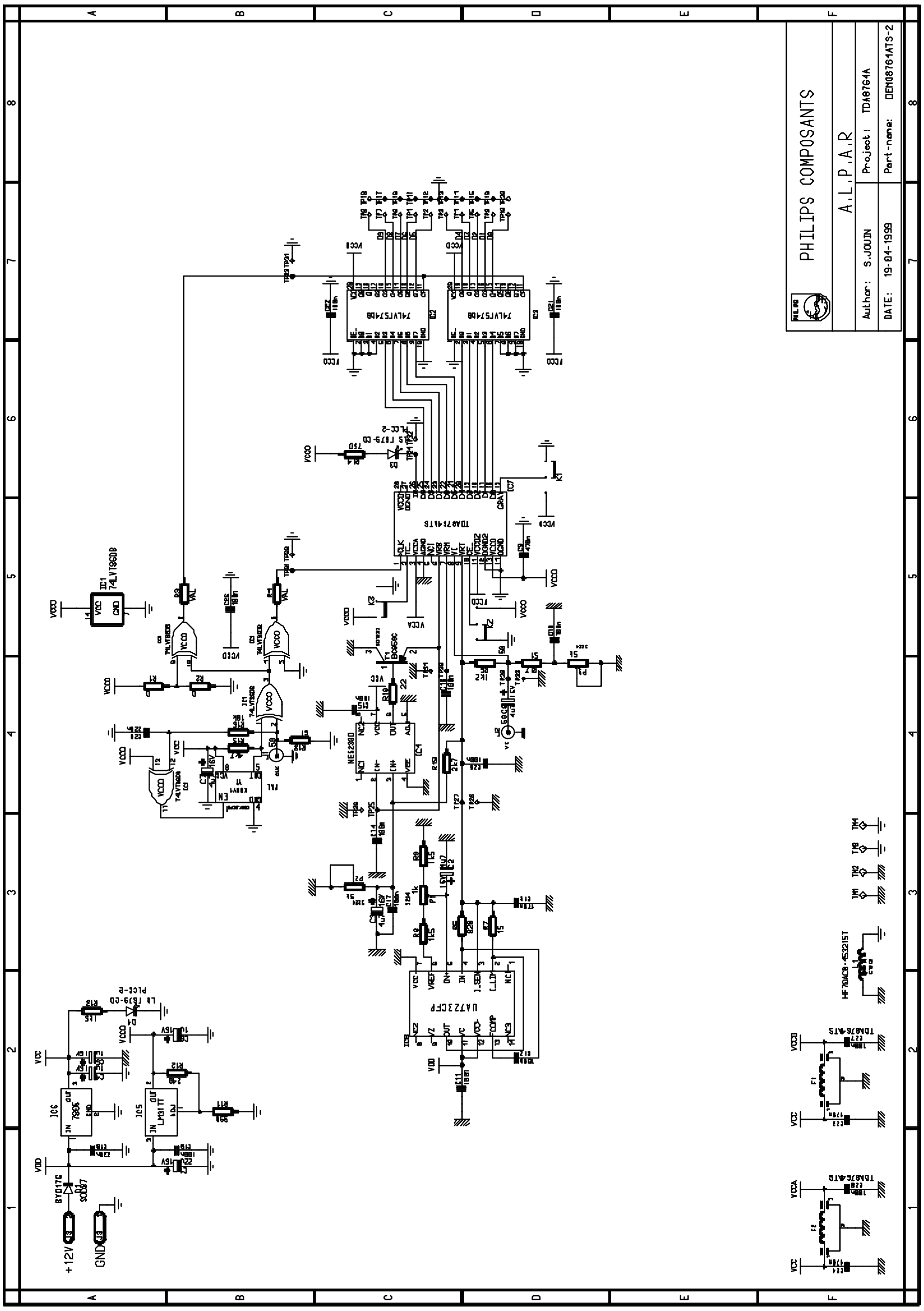
9.1 TDA8764ATS SSOP28 VERSION:

All documents needed for the realization of this Demoboard are given on **Figures 23 to 30**.

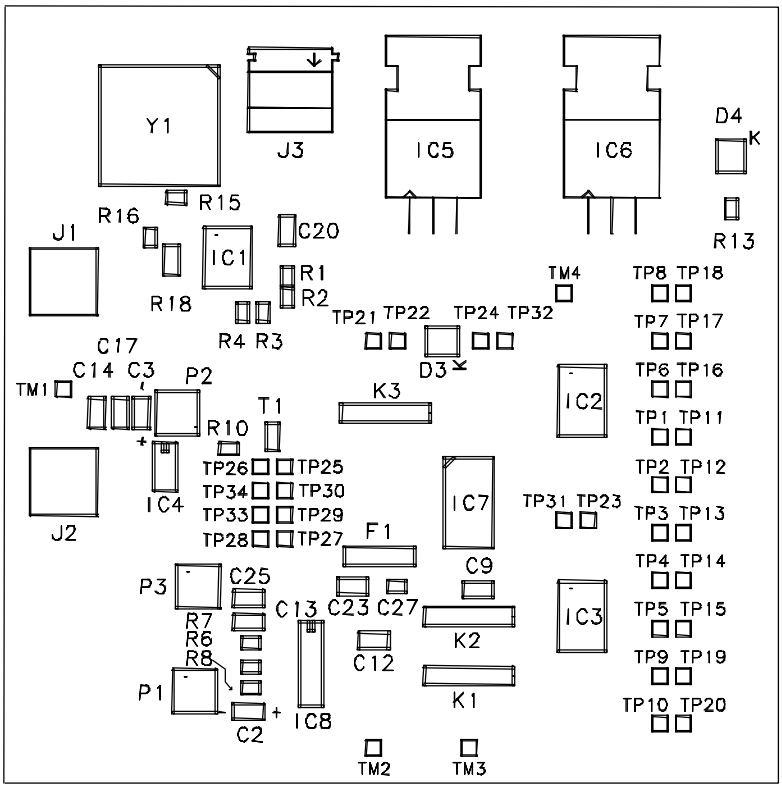
- Electrical diagram.
- Topside component implantation.
- Underside component implantation.
- Topside component layout 1.
- Internal ground plane layout 2.
- Internal supply layout 3.
- Internal ground plane layout 4.
- Underside component layout 5.

9.2 COMPONENTS LIST:

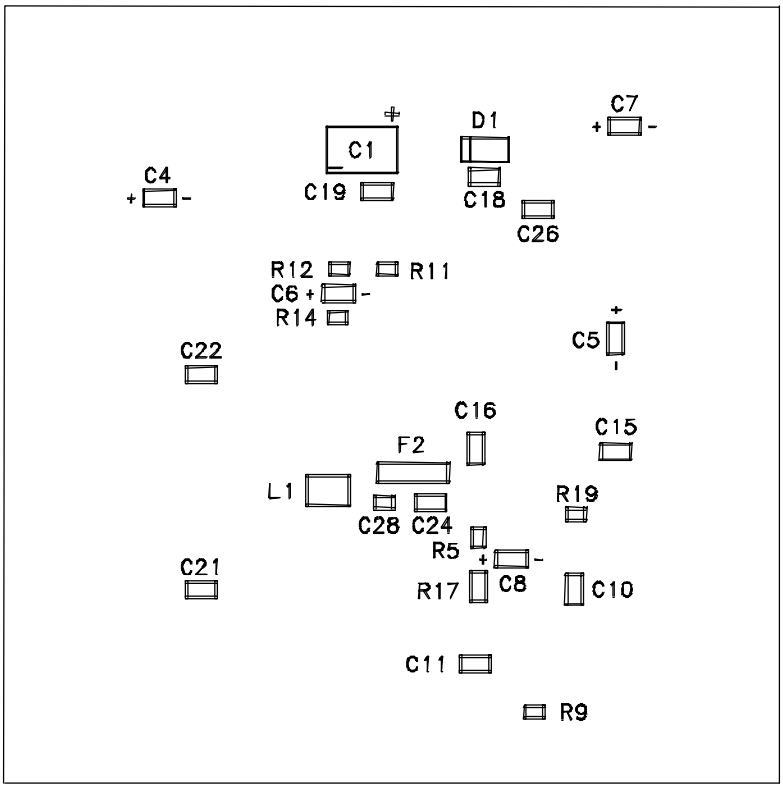
The all version components list with their values and references is given on **Tables 5 to 8**.



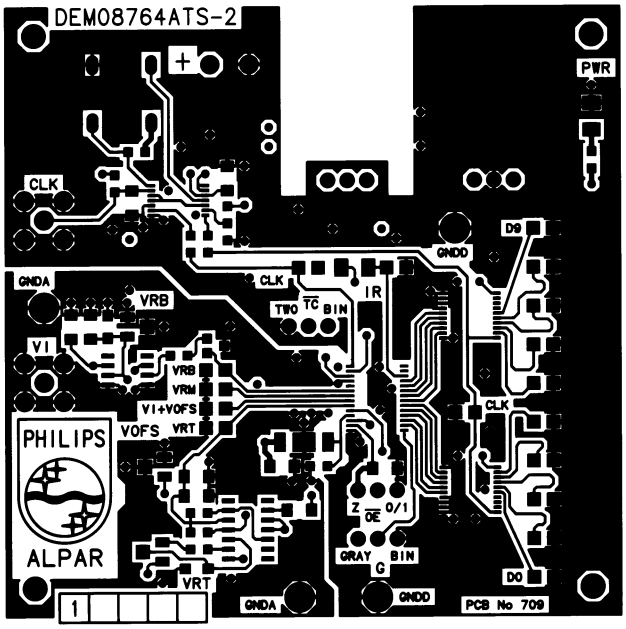
- Figure 23. TDA8764ATS Demoboard electrical diagram -



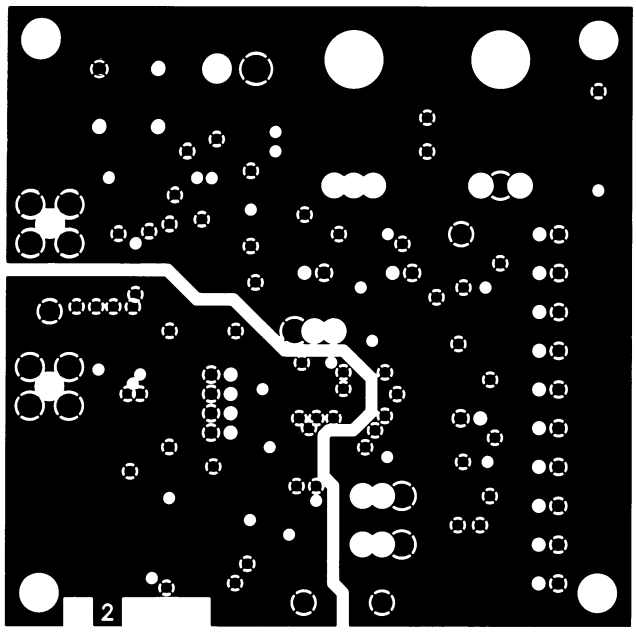
- Figure 24. TDA8764ATS topside component implantation -



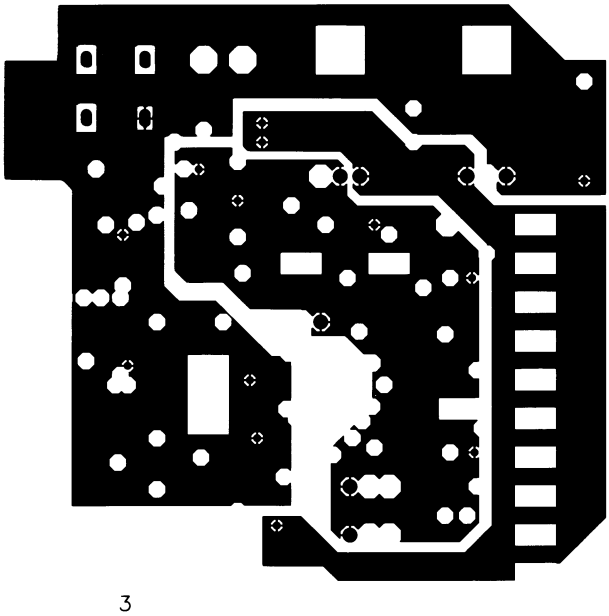
- Figure 25. TDA8764ATS underside component implantation -



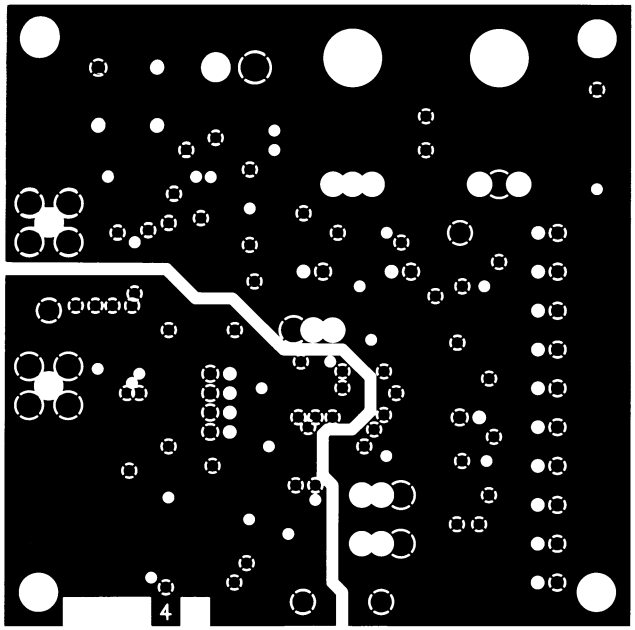
- Figure 26. Topside component layout (signal layer 1) -



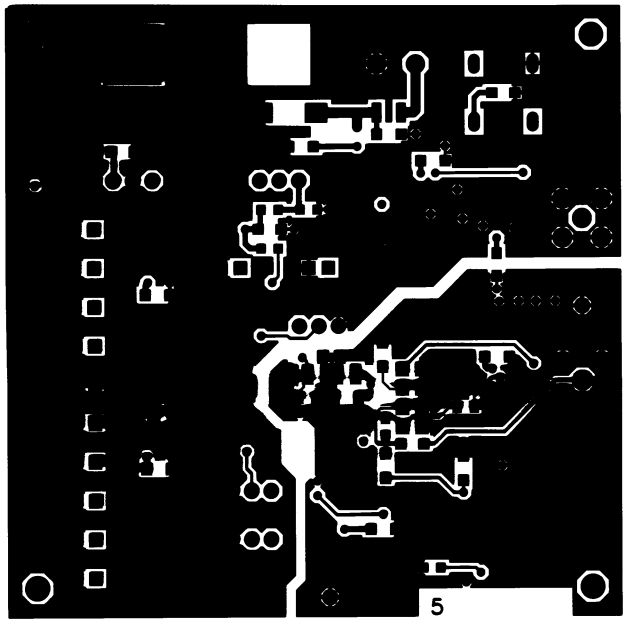
- Figure 27. Internal plane layout (ground layer 2) -



- Figure 28. Internal layout (supply layer 3) -



- Figure 29. Internal plane layout (gound layer 4) -



- Figure 30. Underside component (signal layer 5) -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
C1	22µF/16V	CAPACITOR	293D/D	SPRAGUE
C2	4.7µF/16V	'	293D/A	'
C3	4.7µF/16V	'	'	'
C4	1µF/16V	'	'	'
C5	1µF/16V	'	'	'
C6	1µF/16V	'	'	'
C7	4.7µF/16V	'	'	'
C8	4.7µF/16V	'	'	'
C9	470nF	'	C1206	PHLIPS
C10	100nF	'	'	'
C11	100nF	'	'	'
C12	100pF	'	'	'
C13	470nF	'	'	'
C14	100nF	'	'	'
C15	100nF	'	'	'
C16	100nF	'	'	'
C17	100nF	'	'	'
C18	330nF	'	'	'
C19	100nF	'	'	'
C20	220nF	'	'	'
C21	100nF	'	'	'
C22	100nF	'	'	'
C23	470nF	'	'	'
C24	470nF	'	'	'
C25	100nF	'	'	'
C26	100nF	'	'	'
C27	100nF	'	C805	'
C28	100nF	'	'	'
D1		DIODE	BYD17G	PHILIPS
D2		RED LED	LST679-CO	SIEMENS
D3		GREEN LED	LGT679-CO	'
F1	2nF	Π FILTER	4700-003-S	TUSONIX
F2	2nF	'	'	'
F3	2nF	'	'	'
IC1		EXCLUSIVE-OR	74LVT86DB	PHILIPS
IC2		D TYPE FLIP FLOP	74LVT574DB	'
IC3		D TYPE FLIP FLOP	74LVT574DB	'
IC4		LOW VOLTAGE OP. AMPLI.	NE5230D	'
IC5		ADJUSTABLE REGULATOR	LM317T	TEXAS INSTRUMENTS

- Table 5. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
IC6		VOLTAGE REGULATOR	T7805CT	MOTOROLA
IC7		ADC	TDA8764ATS	PHILIPS
IC8		PRECISION VOLTAGE REG	UA723CD74LVT86DB	'
J1		CONNECTOR	MKSD	PHOENIX
J2	50Ω	CONNECTOR	SMA	RADIALL
J3	50Ω	'	'	'
K2		SWITCH	1C2P	SECME
K4		'	'	'
K5		'	'	'
L1		HF70ACB-453215T	C1812	PHILIPS
P1	1KΩ	POTENTIOMETER	3224W	BOURNS
P2	5KΩ	'	'	'
P3	5KΩ	'	'	'
Y1	40MHz/80MHz	OSCILLATOR	IQX0	KONY
R1	**Do not solder**	RESISTOR	0805	PHILIPS
R2	0Ω	'	'	'
R3	33Ω	'		'
R4	51Ω	'	'	'
R5	1.2kΩ	'	'	'
R6	820Ω	'	'	'
R7	15Ω	'	'	'
R8	1.5kΩ	'	'	'
R9	1.5kΩ	'	'	'
R10	22Ω	'	'	'
R11	390Ω	'	'	'
R12	240Ω	'	'	'
R13	1.5kΩ	'	'	'
R14	750Ω	'	'	'
R15	4.7kΩ	'	'	'
R16	10kΩ	'	'	'
R17	51Ω	'	1206	'
R18	51Ω	'	'	'
R19	2.7kΩ	'	805	'
T1		TRANSISTOR PNP	BC859C	PHILIPS

- Table 6. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
TM1		MEASUREMENT POINT		COMATEL
TM2		'		'
TM3		'		'
TM4		'		'
TP1		TEST POINT		COMATEL
TP2		'		'
TP3		'		'
TP4		'		'
TP5		'		'
TP6		'		'
TP7		'		'
TP8		'		'
TP9		'		'
TP10		'		'
TP11		'		'
TP12		'		'
TP13		'		'
TP14		'		'
TP15		'		'
TP16		'		'
TP17		'		'
TP18		'		'
TP19		'		'
TP20		'		'
TP21		'		'
TP22		'		'
TP23	**Do not solder**	'		'
TP24		'		'
TP25		'		'
TP26		'		'
TP27		'		'
TP28		'		'
TP29		'		'
TP30		'		'
TP31	**Do not solder**	'		'
TP32		'		'
TP33		'		'
TP34		'		'

- Table 7. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
TP10		TEST POINT		COMATEL
TP11		'		'
TP12		'		'
TP13		'		'
TP14		'		'
TP15		'		'
TP16		'		'
TP17		'		'
TP18		'		'
TP19		'		'
TP20		'		'
TP21		'		'
TP22		'		'
TP23		'		'
TP24		'		'
TP25		'		'
TP26		'		'
TP27		'		'
TP28		'		'
TP29		'		'
TP30		'		'
TP31		'		'
TP32		'		'
TP33		'		'
TP34		'		'

- Table 8. List of components -