T/R Switch for IMT-2000 Handset Applications

Alpha

APN1008

Introduction

IMT-2000, International Mobile Technology-2000, is the third generation technology standard developed by the International Telecommunications Union (ITU) for global mobile communications. The spectrum allocation for IMT-2000 is 1885–1980 MHz for up-link (mobile to base station) communication and 2110–2170 MHz for down-link (base station to mobile) communication.

In Europe, the system is known as UMTS. The spectrum allocation is 1920–1980 MHz (up-link) and 2110–2170 MHz (down-link) for Frequency-Division Duplex (FDD) and 1900–1920 MHz and 2010–2025 MHz for Time Division Duplex (TDD).

Wideband CDMA (WCDMA) is the access technology adapted by major Japanese mobile manufacturers and is incorporated in UMTS. Figure 1 shows frequency allocation schemes adapted or under consideration in different parts of the world.

This application note addresses a handset T/R switch design that enables its antenna to be electronically connected to either the transmitter or receiver. It covers both the1885–1980 MHz transmit band (up-link) and the 2110–2170 MHz receive band (down-link). Since the T/R switch is placed at the RF front end of the handset, it has significant influence on transmitter efficiency, receiver sensitivity, and battery consumption. An important characteristic of the RF system is transmit signal linearity and purity which strongly affects the level of interference from neighboring channels. The design demonstrates a high performance T/R switch appropriate for IMT-2000 handset applications utilizing low cost Alpha SMP1320-079 and SMP1320-017 PIN diodes as switching elements.

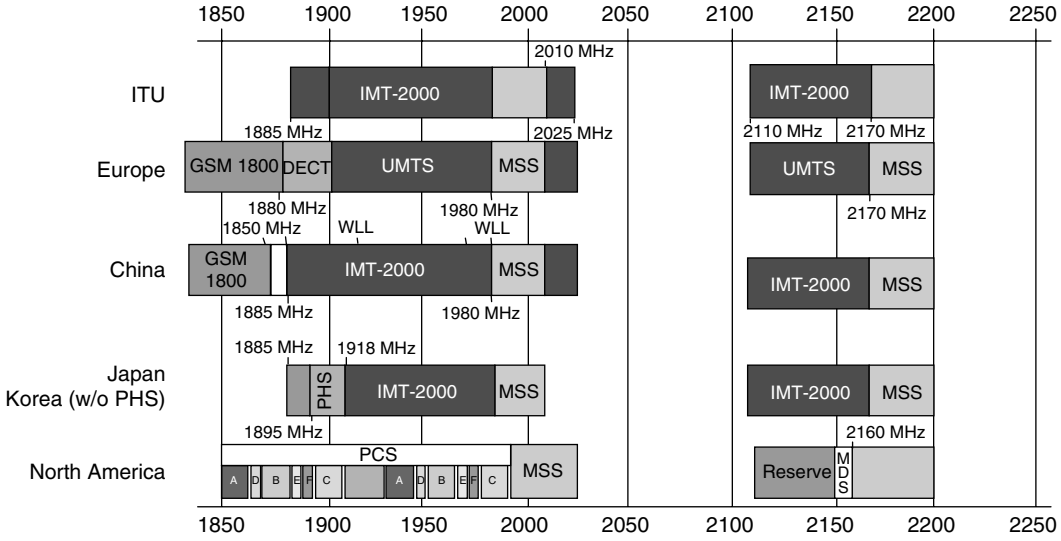


Figure 1. WCDMA Spectrum Allocation by Regions[1]

PIN Diode T/R Switch Fundamentals

The traditional PIN diode based T/R switch is an attractive design option for a handset. The design consists of a series-connected PIN diode placed between the transmitter power amplifier and antenna, and a shunt-connected PIN diode connected at the receiver port, which is a quarter wavelength from the antenna, as shown in Figure 2. When the transmitter is on, forward current is applied to both diodes (low impedance state), allowing low insertion loss between transmitter and antenna. The low impedance of the receiver diode protects it from the transmitter power and the quarter wavelength line transforms the low impedance to high impedance at the antenna port. When the receiver is on, the PIN diodes are at zero bias (high impedance state). This results in low loss between the antenna and the receiver and isolates the off-transmitter. A desirable feature of this handset switch design is that no battery power is consumed in standby when the receiver is on.

For good switch performance, the PIN diodes utilized should have low capacitance at zero bias and low resistance at low forward current. The SMP1320 series, typically 0.35 pF and 2 Ω at 1 mA, was chosen. Low inductance is required for the shunt connected diode so the four lead, SOT-143, SMP1320-017 was chosen. This device has an effective inductance of approximately 0.2 nH. For the series connected diode, the inductance is less critical so the SC-79 package, SMP1320-079, was selected.

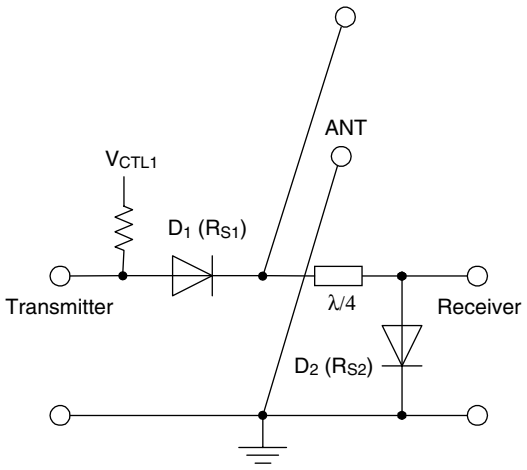


Figure 2. Typical SPDT Switch Design

Circuit Model

In the Libra Series IV model shown in Figure 3, PIN diode, X_4, is the series connected diode in the transmit path and PIN diode, X_3, is connected in shunt in the receive RF path. DC bias is provided through a choke formed by microstrip line, TL_{11}, and capacitor, SRLC11. The 3 V DC supply current is limited to about 5–6 mA by resistor R_2 = 510 Ω.

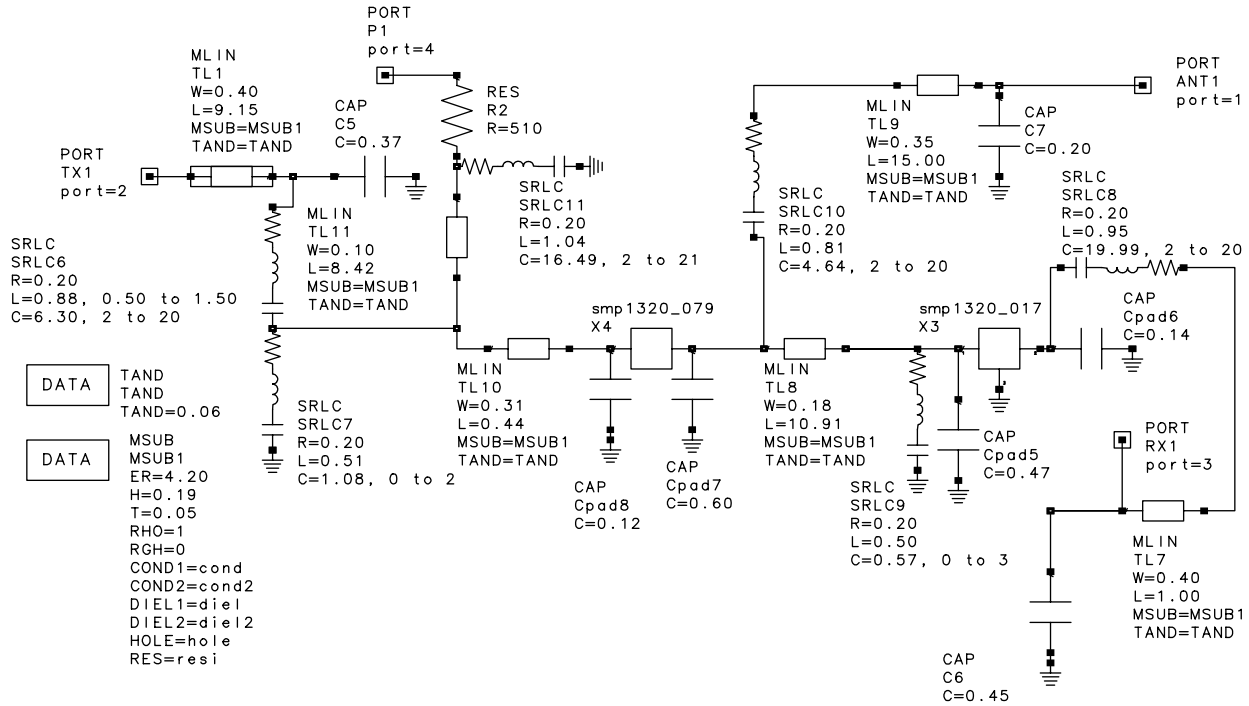


Figure 3. Libra Switch Model

Microstrip line, TL_8, transforms the inductive impedance of the forward biased PIN diode, X_3, to a value high enough not to significantly affect the transmission path. Capacitor, SRLC, modeled as a series R-L-C, tunes out discontinuities caused by the high impedance of transformed TL_8 and PIN diode, X_3, in the receive path.

The low value of the antenna coupling capacitor, SRLC10 (4.64 pF), is modeled as a series connected R-L-C. It resonates in series with its inductance as well as the residual inductances from both the microstrip-coaxial interface and the switch circuit. A higher value of this capacitor should not harm the receive path, but it may significantly degrade the transmit path by moving its pass window to a higher frequency.

Capacitor, SRLC7, also performs a tune-out function, compensating for the inductance of series PIN diode, X_4, and any associated capacitive contributions from placement pads Cpad7, Cpad8, etc. The capacitances formed by the components' placement pads are modeled as discrete capacitors, Cpad5, Cpad6, Cpad7 and Cpad8. Capacitors, C_5, C_6 and C_7 model the discontinuity effects of the microstrip-to-coaxial interface.

Most of the circuit model values were established as a result of a parameter extraction procedure which was used to fit the simulated S-parameters of the initial design with the measured values used in the actual design. More details of this procedure will be discussed in following paragraphs.

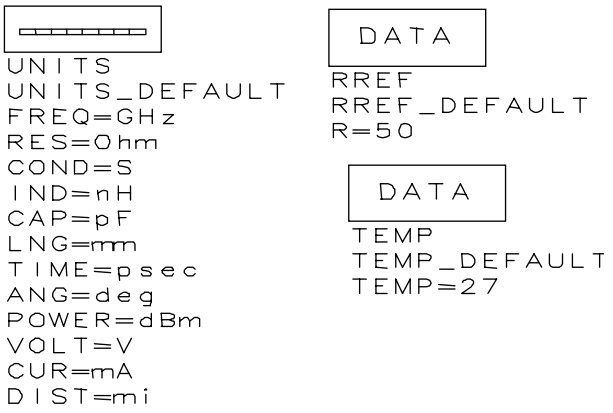


Figure 4. Default Bench Values

SMP1320-079 and SMP1320-017 Models

Alpha's SMP1320 series are silicon PIN diodes designed with typical I region thickness of 8 um and carrier lifetime of 0.4 us. The devices exhibit a wide range of resistance vs. current and are capable of operating with low distortion as a switching element.

The SMP1320-017 lead configuration for the SOT-143 was designed for low inductance in shunt connected diode connections. To be effective the device must be inserted with each anode contact attached to either side of a gap in a microstrip trace with separate ground contacts as shown in Figure 5. With no DC current in Dpin, the diode is at high impedance and the RF current, Ish, is minimal. The RF input current flows directly to the output, Iout. Parasitic inductances, L_1 and L_2, formed by the bond wires and the package leadframe result in about 2–2.5 nH total inductance in the Iout current path.

When diode Dpin is forward biased, the shunt current Ish is high. The voltage drop between the anode of Dpin and ground is due to the small (0.2 nH) inductance of the lead and the PCB via. This small shunt impedance causes the through-current, Iout, to be relatively small and allows the PIN diode to provide useful attenuation of frequencies beyond 6 GHz.

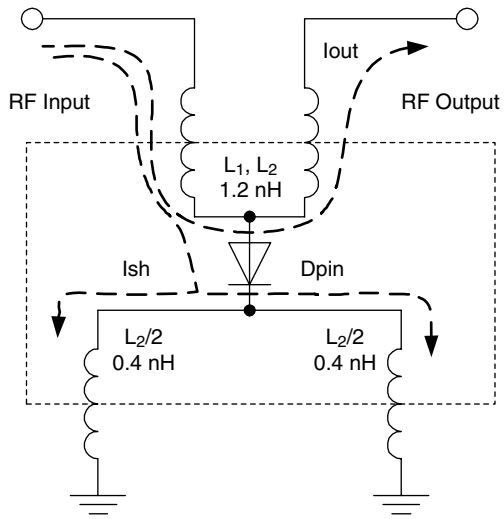


Figure 5. Low Inductance SOT-143

Models for the SMP1320-017 and SMP1320-079 PIN diode defined for the Libra IV environment are shown in Figures 6a and 6b with a description of the parameters used. In each model, two diodes were used to fit both the DC and the RF properties of each PIN diode. The PIN diode built-in model of Libra IV is used to model behavior of RF resistance vs. DC current. The PN-junction diode model was used to model the DC voltage-current characteristic. Since both diodes are connected in series, the same DC current flows through both. In the PN-junction model, the diodes are effectively RF shorted with capacitor C_2 set at 10^{11} pF. The portion of the RF resistance that reflects a residual series resistance was modeled as R_2 = 0.8 Ω. This resistor is connected in parallel with ideal inductor, $L_1 = 10^{19}$ nH, thus it has zero Ω at DC. Capacitors C_G, and C_P, and inductor L_2 reflect the junction and package properties of SMP1320 diodes. The exact inductance and capacitance values of the package and diode junction were trimmed to best fit simulated and measured results of the working switch circuit. The reason for trimming is to improve the accuracy of the model in the WCDMA frequency range caused by the interaction of package parasitics and board layout.

The linear model that emulates the DC and RF properties of the PIN diode is described in Reference 3. The fundamental properties of PIN diodes are described in Reference 2.

Tables 1 and 2 display the model parameters for a silicon PIN diode and a silicon PN diode. They show the default values appropriate for silicon diodes that may be used by the Libra IV simulator. Some values of the built-in PIN diode model of Libra IV were not used. These are marked “not used” in the tables.

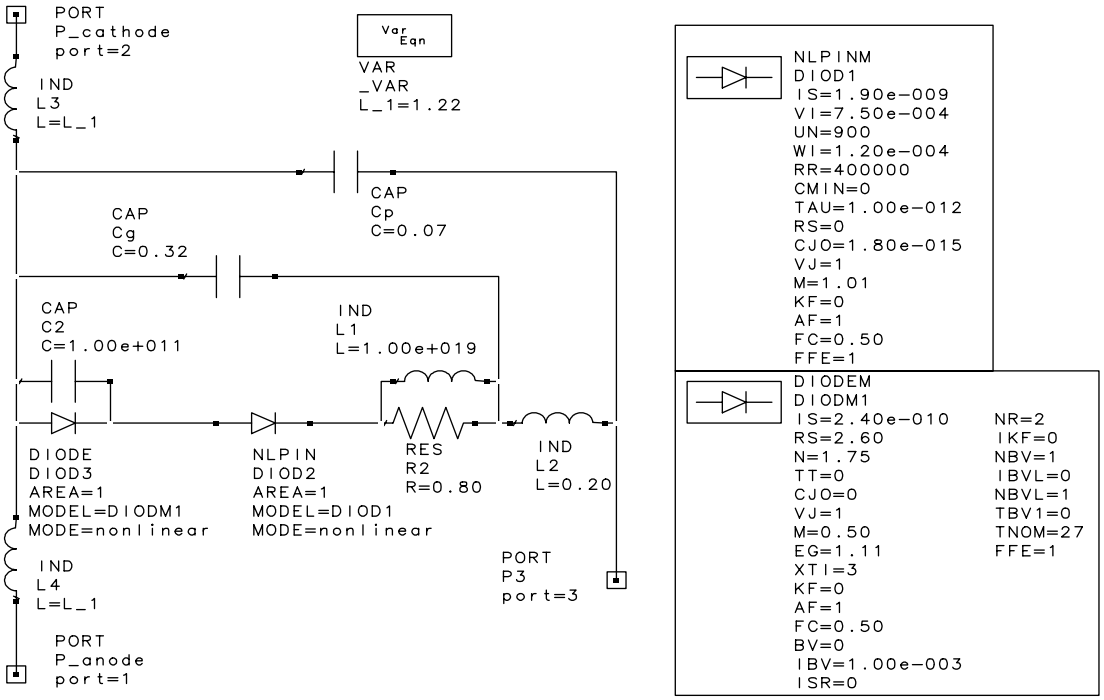


Figure 6a. SMP1320-017 Small Signal Model

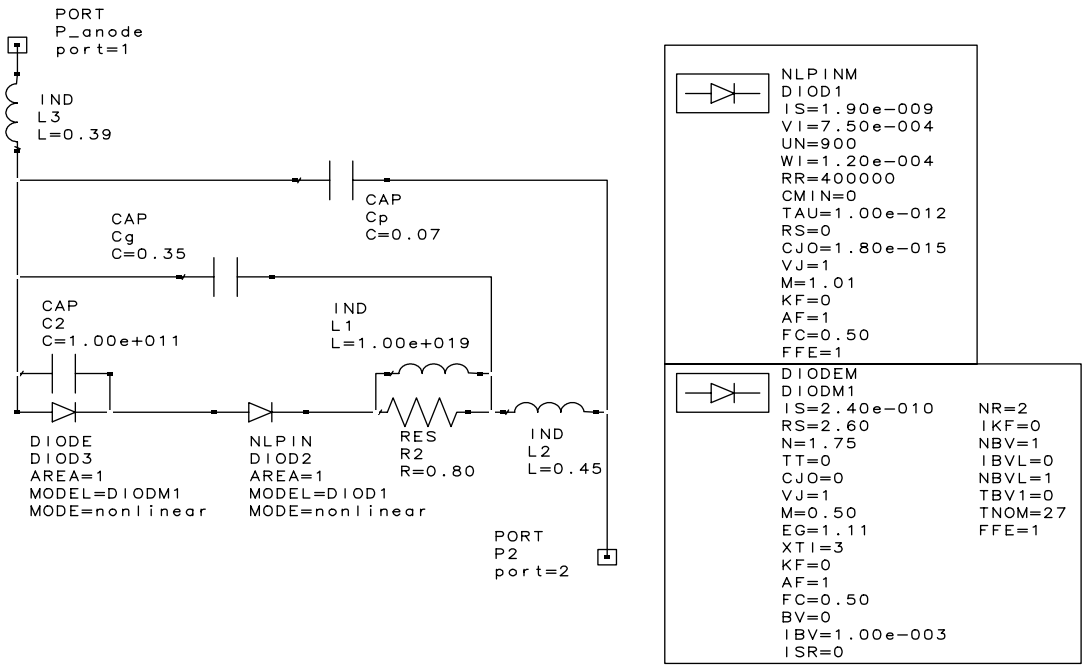


Figure 6b. SMP1320-079 Small Signal Model

Parameter	Description	Unit	Default SMP1320
IS	Saturation current (Not used)	A	1.9E-9
VI	I region forward-bias voltage drop	V	7.5e-4
UN	Electron mobility cm**2/(V*S) (Not used)	cm**2/(V*S)	900
WI	I region width (Not used)	M	1.2e-4
R_R	I region reverse-bias resistance	Ω	4E5
C_{MIN}	PIN punchthrough capacitance	F	0
TAU	Ambipolar lifetime within I region (Not used)	S	1E-12
R_S	Ohmic resistance	Ω	0
C_{JO}	Zero-bias junction capacitance	F	1.8E-15
V_J	Junction potential	V	1
M	Grading coefficient	-	1.01
KF	Flicker-noise coefficient (Not used)	-	0
AF	Flicker-noise exponent (Not used)	-	1
FC	Coefficient for forward-bias depletion capacitance (Not used)	-	0.5
FFE	Flicker-noise frequency exponent (Not used)	-	1

Table 1. Silicon PIN Diode Values in LIBRA IV Assumed for SMP1320 Models

Parameter	Description	Unit	Default SMP1320
IS	Saturation current	A	2.4E-10
R_S	Series resistance	Ω	2.6
N	Emission coefficient (Not used)	-	1.75
TT	Transit time (Not used)	S	0
C_{JO}	Zero-bias junction capacitance (Not used)	F	0
V_J	Junction potential (Not used)	V	1
M	Grading coefficient (Not used)	-	0.5
E_G	Energy gap (with XTI, helps define the dependence of IS on temperature)	EV	1.11
XTI	Saturation current temperature exponent (with E_G, helps define the dependence of IS on temperature)	-	3
KF	Flicker-noise coefficient (Not used)	-	0
AF	Flicker-noise exponent (Not used)	-	1
FC	Forward-bias depletion capacitance coefficient (Not used)	-	0.5
B_V	Reverse breakdown voltage (Not used)	V	Infinity
I_{BV}	Current at reverse breakdown voltage (Not used)	A	1e-3
ISR	Recombination current parameter (Not used)	A	0
NR	Emission coefficient for ISR (Not used)	-	2
IKF	High-injection knee current (Not used)	A	Infinity
NBV	Reverse breakdown ideality factor (Not used)	-	1
IBVL	Low level reverse breakdown knee current (Not used)	A	0
NBVL	Low level reverse breakdown ideality factor (Not used)	-	1
T_{NOM}	Nominal ambient temperature at which these model parameters were derived	°C	27
FFE	Flicker-noise frequency exponent (Not used)		1

Table 2. Silicon PN Diode Values in LIBRA IV Assumed for SMP1320 Models

Circuit Design Procedure

Because the transmit and receive frequency bands of IMT-2000 are separated, an iterative design procedure (shown in Figure 7) was used to optimize performance. Under model parameters, values were established for most of the parasitic components such as the capacitance of landing pads, transition discontinuities, inductances of the discrete capacitors, and connection lines (refer to the circuit model in Figure 3). In the initial stage, many of these model parameters could not be defined because of layout uncertainty. A round of simulation was performed to resolve this uncertainty and establish the circuit layout. In this round the basic circuit, transmission lines, and capacitances were defined, resulting in the PCB layout shown in Figure 9.

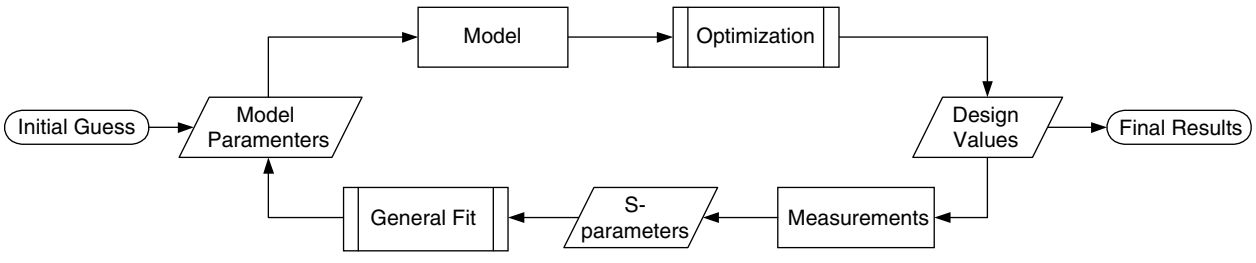


Figure 7. T/R Switch Iterative Design Chart

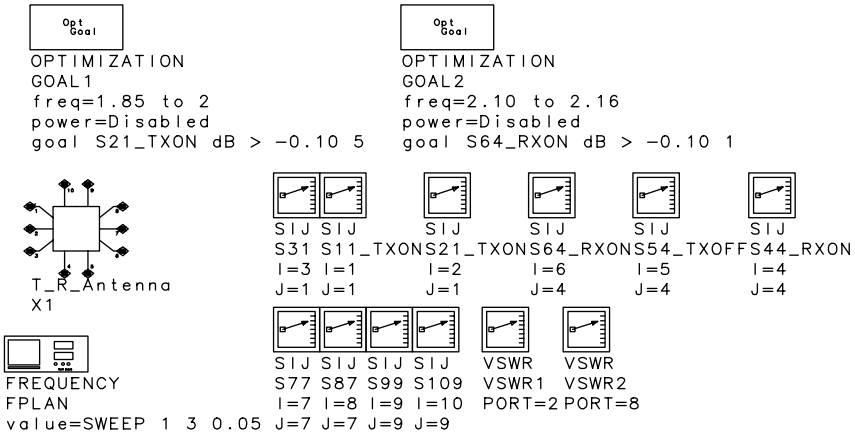


Figure 8. Test Bench Defining "Optimization" Design Goals

The optimization process goals, in Figure 7, are defined in the test bench design shown in Figure 8. Here GOAL1 minimizes insertion loss in the up-link frequency band, and GOAL2 minimizes the insertion loss in the down-link frequency band. Both Transmitter_ON and Receiver_ON states of the switch are defined on the single circuit test bench by consecutively applying either +3 V or 0 V to the bias port of the switch model in Figure 3. In Figure 10, the ports of the T_R_Antenna module are defined.

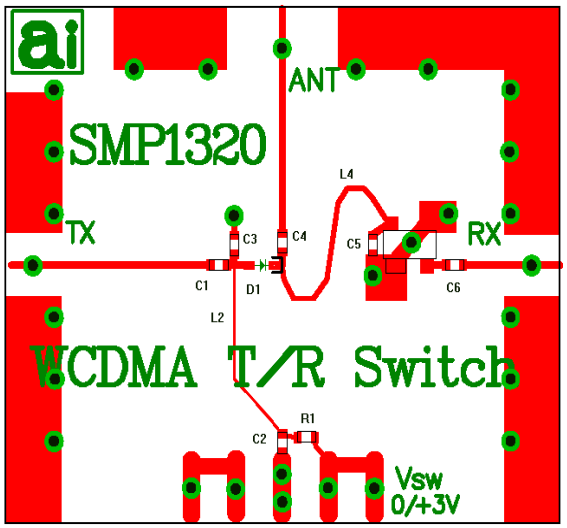


Figure 9. PCB Layout

Ideally, the optimization parameters in the design stage include varying the lengths and widths of transmission lines TL_8 and TL_{11}, as well as the capacitor values in Figure 3, defined as constraint variable parameters. However, the layout was not intended to be redone after it was fixed during the initial simulation run. Therefore, the design iteration cycles did not allow the geometries of TL_8 and TL_{11} to change.

In the IMT-2000 frequency range, the contribution of multiple parasitic components could not be ignored and required consecutive circuit trimming. These parasitic components include both direct circuit layout contributors and transitions from microstrip to coax. In addition, when comparing simulation results with measured S-parameters, the reference plane shift should be taken into account. In Figure 10, the reference plane shift is described by ideal transmission lines, TL_1–TL_4.

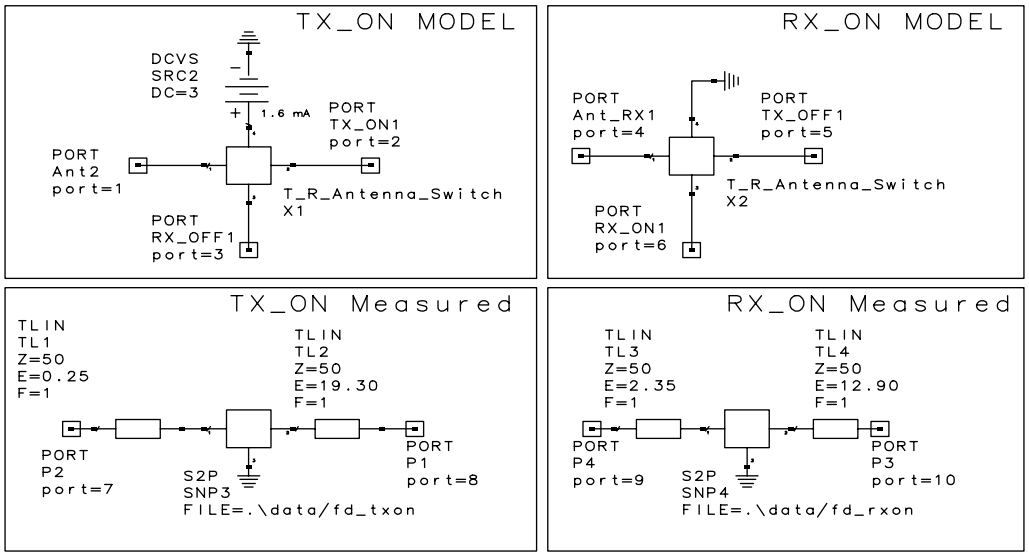


Figure 10. T/R Antenna Module Circuit Model

The general fit process in Figure 7 signifies an optimization procedure to minimize the difference between measured and simulated S-parameters in both Transmit_ON and Receive_ON states. Most of the parasitic and transmission line parameters were allowed to vary within reasonable ranges. To avoid additional complications, many discontinuity models were simplified as LC networks with lumped elements, whose parameters were considered independent variables in the fitting procedure. These simplifications resulted in some model components differing from physically measurable parameters (e.g. transmission line width or length). In addition, we allowed package inductances and capacitances of the PIN diode to be modified by the fitting process.

The goal functions for the fitting procedure are described on the test bench in Figure 11. The circuit model for the T_R_Antenna_Fit module was similar to that shown in Figure 10, except that the line lengths of TL_1–TL_4 were allowed to change in the range of 0–15°.

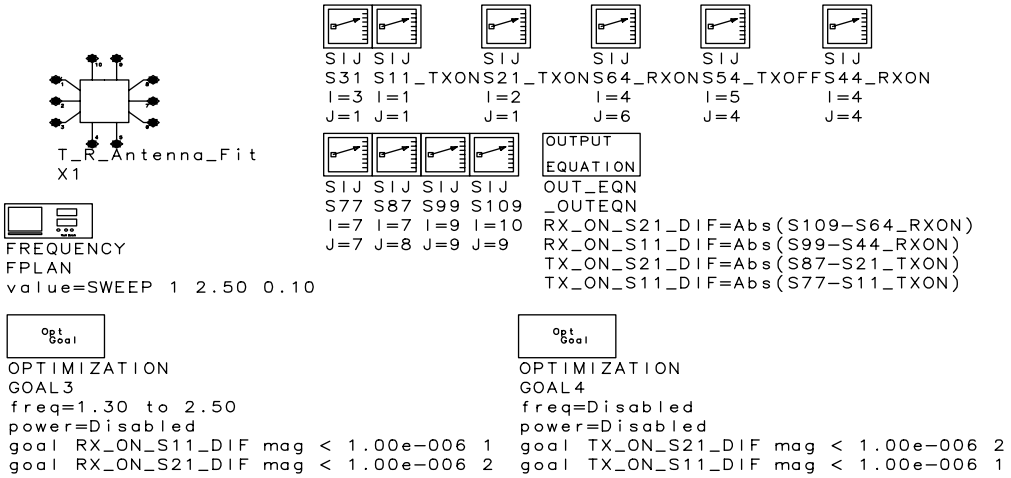
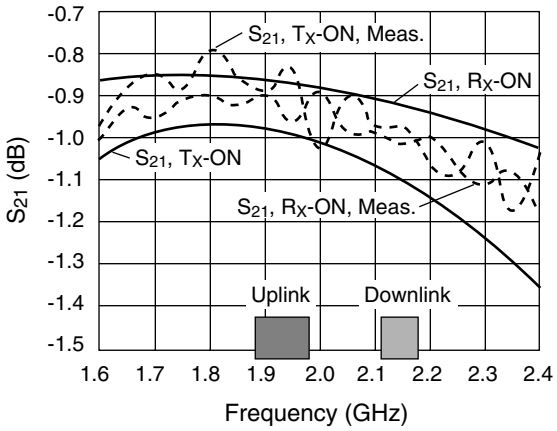


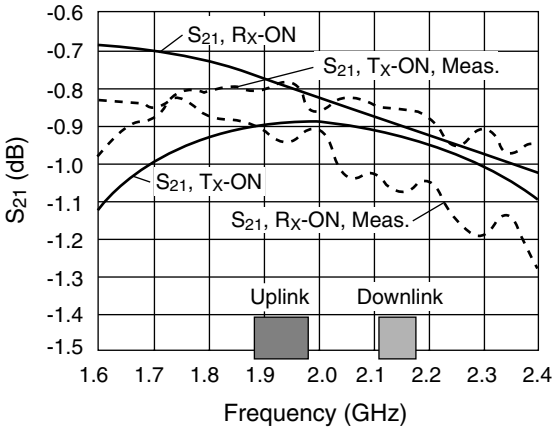
Figure 11. Fitting Procedure Test Bench

When the fitting function reached it's minimum, the optimized parameters were entered into the modified switch circuit model (Figure 3). The optimization design process was then repeated to further improve circuit performance. After each iteration, the modified circuit values were installed and a new set of S-parameters was measured. This iterative process continued until no further significant performance improvement was achieved.

This circuit required three design iterations to achieve the desired performance. Figures 12a and 12b show the results of two consecutive design iterations. Figure 12b shows the circuit component values used in the last iteration of Figure 13 and in the bill of materials shown in Table 3.



12a



12b

Figures 12a and 12b. Measured and Simulated T/R Switch Insertion Losses for Two Consecutive Design Iterations

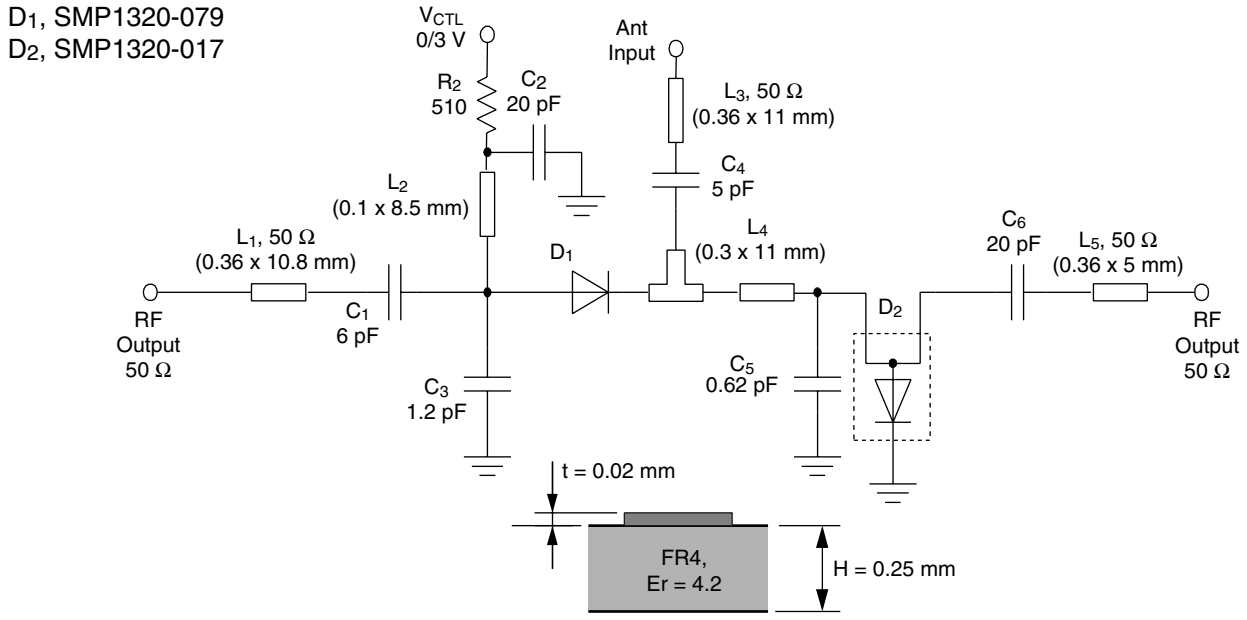


Figure 13. T/R Switch Circuit Diagram

Designator	Value	Part Number	Footprint	Manufacturer
C_1	6 p	CM05CG6R0K10AB	0402	AVX/KYOCERA
C_2	20 p	CM05CG200K10AB	0402	AVX/KYOCERA
C_3	1.2 p	CM05CG1R2K10AB	0402	AVX/KYOCERA
C_4	5 p	CM05CG5R0K10AB	0402	AVX/KYOCERA
C_5	0.6 p	CM05CG0R6K10AB	0402	AVX/KYOCERA
C_6	20 p	CM05CG200K10AB	0402	AVX/KYOCERA
R_1	510	CR05-511J-T	0402	AVX
D_1	SMP1320-079	SMP1320-079	SC-79	ALPHA Industries
D_2	SMP1320-017	SMP1320-017	SOT-143	ALPHA Industries
L_1	0.36 x 10.8 mm	MSL, 50 Ω	0.36 x 10.8 mm	(printed on PCB)
L_2	0.1 x 8.5 mm	MSL	0.1 x 8.5 mm	(printed on PCB)
L_3	0.36 x 11 mm	MSL, 50 Ω	0.36 x 11 mm	(printed on PCB)
L_4	0.3 x 11 mm	MSL	0.3 x 11 mm	(printed on PCB)
L_5	0.36 x 5 mm	MSL, 50 Ω	0.36 x 5 mm	(printed on PCB)

Table 3. Bill of Materials for the T/R Switch

Circuit and Layout Description

The circuit diagram for the switch is shown in Figure 13 and the PC board layout is shown in Figure 9. The bill of materials for the switch is shown in Table 3.

The PC board is made of 0.25 mm thick, standard FR4 material metalized with two-sided 0.02 mm thick copper. In the test board the RF signals were fed through SMA connectors.

Line L_4 was meandered to reduce the active board area. Continued meandering of lines L_2 and L_4 was not done because accurate models were not available to predict performance.

Three via holes were used as ground pins for PIN diode, D_2, to reduce common mode inductance.

Switch Performance

Measured switch performance is shown in Figures 14 and 15. The insertion loss in the transmit (up-link) state, measured at V_{CTL} = 3 V (1.8 mA), was less than 0.85 dB; the insertion loss in the receive (down-link) state, at V_{CTL} = 0 V, was less than 1.1 dB. The higher receive state insertion loss was due to the design goal preference, which favored transmit state insertion loss (see Figure 8). In the model, circuit loss was referenced to the input point of DC blocking capacitors C_1, C_4, and C_6. This probably resulted in an additional 0.15 dB loss, shown in Figure 14, due to loss in the board interface circuitry.

A simulation analysis shows that the largest contributor to insertion loss (both in transmit and receive paths) is the PCB substrate. This includes metal losses, which have an effective loss tangent of 0.06, contributing up to 0.5 dB to the total loss. An additional 0.1 to 0.2 dB loss in the transmit path is due to the residual resistance of the switching diode. In the receive state, the capacitance of the series diode has a large impact. This decreases the capacitance of the series PIN diode from 0.42 pF to 0.22 pF and decreases the loss by 0.15 dB.

The transmit, up-link, state receiver isolation, and SWR are shown in Figure 15. In this band the SWR was about 1.15 and the isolation was better than 28 dB. The receiver isolation showed a strong function of common mode inductance in the shunt diode (L_2 in Figure 6a). A change of inductance from 0.2 to 0.4 nH would cause more than 5 dB degradation in isolation.

Intermodulation distortion measurements were performed in both transmit and receive states. In the transmit state at 3 V V_{CTL}, (1.8 mA) a third order intercept point (IP3) of +63 dBm was measured. Two signals, each at +34 dBm, were applied to the transmitter port and distortion was measured at the antenna port with the receiver port terminated. However, the measurement system baseline IP3 was about +68 dBm making the actual IP3 better than the measured +63 dBm.

The distortion calculation, according to Reference 5, computed an IP3 of +68 dBm for an SMP1320 PIN diode switch. IP3 values higher than +60 dBm are more achievable with GaAs MESFET switches.

In the receive state, distortion was measured at IP3 = 35 dBm. This measurement was made using two signals, each at +20 dBm applied to the antenna port and measured at the receiver port with the transmitter port terminated.

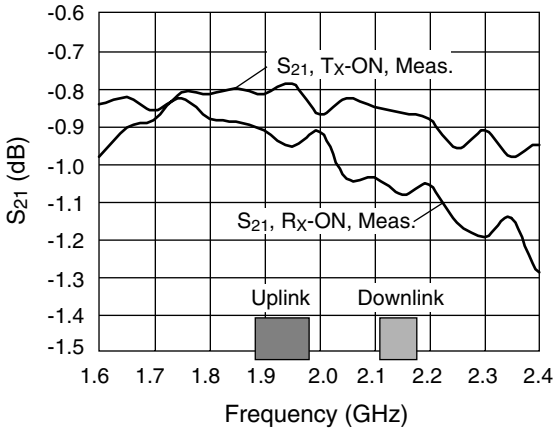


Figure 14. Transmit (ON) and Receive (ON) Insertion Loss

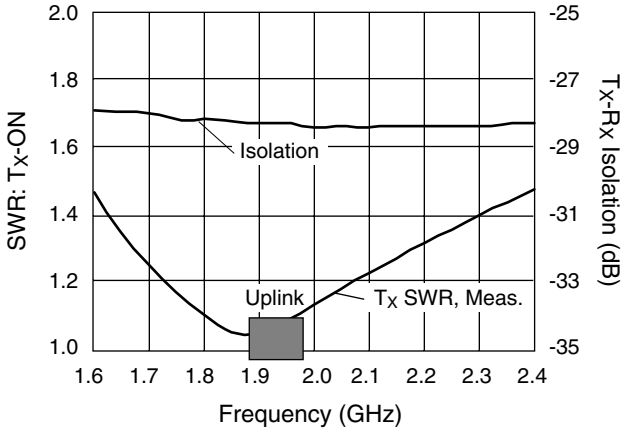


Figure 15. Measured: SWR and T_X-to-R_X Isolation in T_X-ON Mode

References

1. "Minimum Spectrum Demand per Public Terrestrial UMTS Operator in the Initial Phase." UMTS Forum Report # 5, September, 1998.
2. Gerald Hiller, "Design with PIN Diodes," Application Note APN1002, Alpha Industries Inc.
3. J. Walston, "Spice Circuit Yields Recipe for PIN Diode," Microwaves and RF, Nov. 1992.
4. Gerald Hiller, "Predict Intercept Points in PIN Diode Switches," Microwaves & RF, Dec. 1985.
5. Robert Caverly and Gerald Hiller, "Distortion in PIN Diode Control Circuits," IEEE Trans. Microwave Theory Tech., May 1987.
6. "A Wideband General Purpose PIN Diode Attenuator," Application Note APN1003, Alpha Industries, 1999.
7. "5.8 GHz Switch Using Plastic Package PIN Diodes," Application Note APN1011, Alpha Industries, 1999.
8. "A CATV Attenuator Using the Single Package SMP1307-027 PIN Diode Array," Application Note APN1007, Alpha Industries, 1999.

List of Available Documents

The T/R Switch Simulation Project Files for Libra IV.

The T/R Switch PCB Gerber Photo-plot Files.