AN1578
APPLICATION NOTE

DEVELOPING ST92F250 APPLICATIONS USING THE ST92F150-EMU2 EMULATOR

by Microcontroller Division Applications

INTRODUCTION

The ST92F150-EMU2 Emulator is built around the ST92F150 device and can be used to emulate any of the family of the ST92F124/F150/F250 devices.

The purpose of this document is to present how to perform ST92F250 emulation using the ST92F150-EMU2.

The first part of this document lists the differences between the ST92F250CV2 and the ST92F150JDV1. The second part evaluates the restrictions that apply when using the ST92F150 emulator to debug a ST92F250 application.

1 ST92F250 VERSUS ST92F150

Table 1. ST92F250CV2 versus ST92F150JDV1

Feature	ST92F150JDV1	ST92F250CV2
Emulation	Yes	No
RAM Size	6 Kbytes	8 Kbytes
Flash Memory Size	128 Kbytes	256 Kbytes
CAN Interfaces	2	1
J1850 (JBLPD) Interface	Yes	No
I2C Interfaces	1	2
SCI-A LIN Master	No	Yes
IO and AS/DS/RW drive	Programmable: Standard or High Drive	Standard: except P46 P47 P64 P65
WKUP6 mapping	P51/RX1	P51
IO reset behavior	Refer to the Errata Sheet	Refer to the Datasheet
A[18:17]	Available	Not Available when the I²C_1 is in use (when I2CCR.PE bit is set).
P30, P66 and P67	No	Yes
AVDD Parasitic Diode	Yes, Refer to the Errata Sheet	No

1.1 SCI-A LIN MASTER

A Local Interconnect Network (LIN) Message Frame starts with a 13-bit Synch Break.

Software LIN Master solutions are based on a standard asynchronous Serial Communication Interface that generates a 10-bit break (continuous dominant low level).

Some software workarounds exist, for instance changing the baud rate before sending a Synch Break, but they have some limitations and they increase the code size. The ST92F250 SCI-A has a hardware feature for generating a 13-bit Synch Break this is possible in LIN Master mode which is entered by setting the LINE bit (bit 6 of the SCICR3 Register, R255 page 26).

1.2 I/O AND AS/DS/RW DRIVE

The high drive option (EMR1.BSZ bit=1) available in the ST92F150 does not exist in the ST92F250. This means that whatever the value of the BSZ bit (bit 1 of the EMR1 register, R245 page 21), the I_{IO} Load Current remains the same.

Table 2. Maximum Load Current I_{IO}I

	EMR1.BSZ=0	EMR1.BSZ=1	
		ST92F150	ST92F250
P4[7:6],P6[5:4]	4mA	16mA	16mA
P0[7:0],P2[3:2], AS,DS,RW	4mA	16mA	4mA
All other pins except OSCOUT	4mA	4mA	4mA

This could impact an application ported from ST92F150 to ST92F250 in terms of external memory access speed (if EMR1.BSZ bit=1 in the application):

– If the application code doesn't modify the reset state of the BSZ bit, the External Memory Interface of the ST92F250 will have the same timing characteristics as the ST92F150.

– If the application code modifies the reset state of the BSZ bit, the External Memory Interface of the ST92F250 will have different timing characteristics from the ST92F150, and the application may have to be adapted by adding some wait cycles (refer to the External Memory Interface Chapter of the datasheet).

1.3 WKUP6 MAPPING

The ST92F120/F124/F150/F250 microcontrollers have a STOP low power mode which can be exited by a Wake-Up event on the INTD1 external interrupt channel. The Wake-Up event can be a rising or a falling event on one of the 16 Wake-Up lines: WKUP[15:0] (Refer to the Wake-Up / Interrupt Lines Management Unit Chapter of the datasheet).

In the ST92F150, the WKUP6 line is connected on both the CAN0 RX line (or P5.1 in standard I/O mode) and the CAN1 RX line. This is a useful feature for applications that use the CAN interfaces since an event on the CAN buses will wake-up the microcontroller.

As the ST92F250 includes only one CAN, the WKUP6 line is connected only to the CAN0-RX (or P5.1 in standard I/O mode) and the pin corresponding to the CAN1 RX line becomes the standard I/O P6.6.

Application Impact: if an ST92F150 application uses the WKUP6 line on the CAN1 RX line, this feature is not available on the ST92F250 and the signal must be connected to another Wake-Up line (or on P5.1 WKUP6).

1.4 NEW P30, P66 AND P67 STANDARD I/O

As the ST92F250 does not include the J1850(JBLD) and the second CAN peripheral, it has three additional standard Input/Output ports:

– The P3.0, replacing the VPWO pin and providing a complete 8-pin P3 port.

– The P6.6 and the P6.7, replacing the CAN1 RX and TX lines and providing a complete 8-pin P6 port.

1.5 FLASH

1.5.1 FLASH Memory Mapping

To extend the FLASH memory size up to 256Kbytes, two 64Kbyte sectors have been added in the ST92F250. These sectors F4 and F5 are mapped in the second and third memory segments.

1.5.2 FLASH & E3 ™ Status Register 0 (FESR0)

The meaning of the four first bits of the FESR0 register (located at the addresses 224002h and 221002h) is modified to indicate the status of all the FLASH sectors.

Bit 6:0 = FESS[6:0]. Flash and E3™ Sectors Status

These bits are set by hardware and give the status of the 7 Flash and E3™ sectors.

For ST92F150 128K and 64K Flash devices:

– FESS3:0 = Flash sectors (F3:0)

For the ST92F250 256K Flash device:

– FESS3 gives the status of F5, F4 and F3 sectors: the combined status of all these three sectors is ORed on this bit.

– FESS2:0 = Flash sectors (F2:0)

1.5.3 NON VOLATILE WRITE PROTECTION REGISTER (NVWPR)

The meaning of bit 3 of the NVWPR register (located at the address 231FFDh) is modified to take the F4 and F5 sectors into account.

Bit 3 = WPRS3: FLASH Sectors 5-3 Write Protection.

This bit, if programmed to 0, disables any write access to Flash sectors F3, F4, and F5.

2 ST92F250 EMULATION

As stated in the previous chapter, an ST92F250 application with the following characteristics can be emulated by a ST92F150 emulator without any restrictions:

– Second I2C not used.

– SCI-A LIN Master feature not used.

– P3.0, P6.6 and P6.7 not used.

– I/O configuration changed in the first step of the application code.

– Application not impacted by the ADC parasitic diode.

In all other cases the differences must be taken into account during the application development using the ST92F150 emulation to anticipate the application behaviour on the ST92F250.

Flash management and the new features (second I2C, SCI-A LIN Master mode and new I/Os) must be validated in the ST92F250 device in the application.

The following ST9 HDS2V2 emulators and emulation probes support upgrades and/or reconfiguration with new probe hardware:

– ST92F150-EMU2

– ST92F120-EMU2

– ST90158-EMU2 and ST90158-EMU2B

– ST92141-EMU2

– ST92163-EMU2

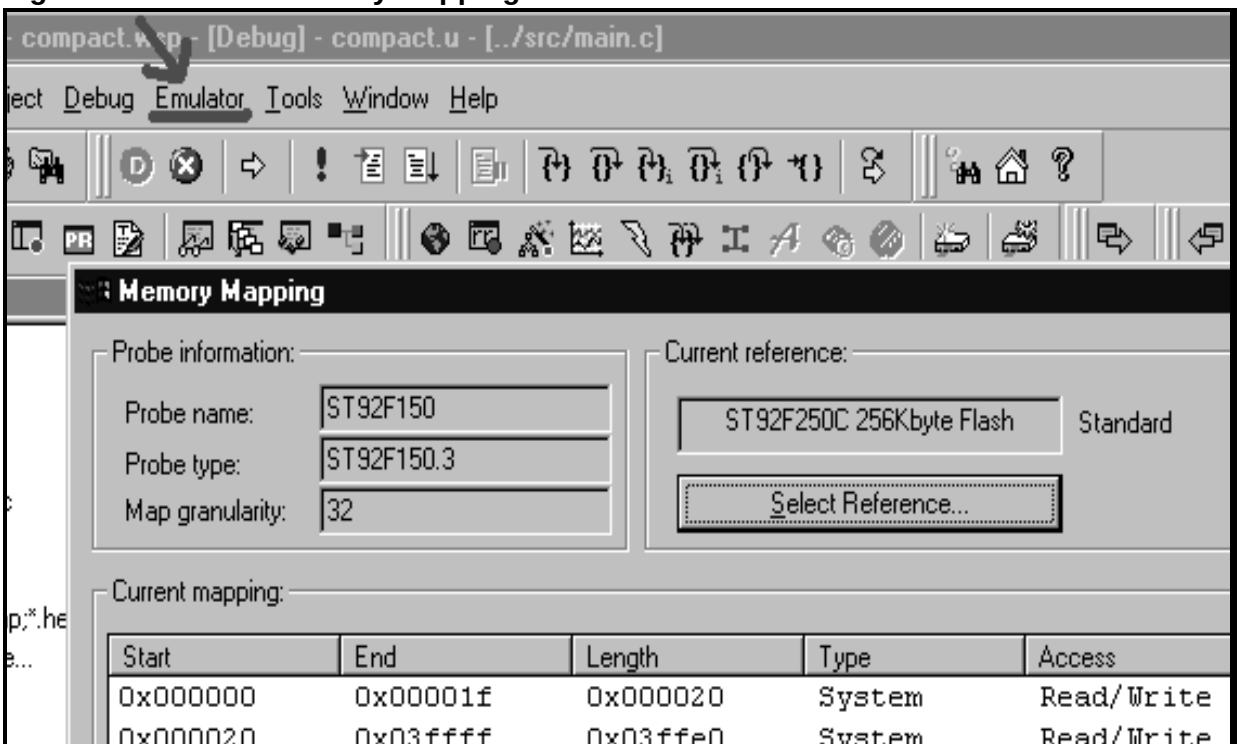
To upgrade a ST92F120 Emulator to a ST92F150 Emulator, refer to application note AN977 Guidelines for upgrading from the ST92F120 (0.50µm) to the ST92F124 and ST92F150 (0.35 µm).

2.1 FLASH AND RAM MEMORY AREAS

The ST9 emulator emulates the internal memory with a RAM memory embedded in the emulator mainboard. All the ST92F250 FLASH and RAM memory areas can be emulated with a ST92F150 emulator, with the limitations due to the RAM and FLASH differences (program and erase process).

To specify the device memory organization, use the Emulator-> Memory Mapping menu, and ST92F250 256Kbyte Flash device.

Figure 1. Emulator Memory Mapping



2.2 SCI-A LIN MASTER

With the ST92F150 emulator, the prescaler must be increased before sending the Synch Break and decreased before sending the Synch Field. For instance:

– Fcpu=24MHz, Normal Prescaler=75, BaudRate=20kbps. BitLength=50us, Synch-Break=500us.

– Fcpu=24MHz, Synch Break Prescaler=95, BaudRate=15.8kbps. BitLengh=63.33us, Break-Length=506us.

The second configuration can be used for the Synch Break generation and the first one for the other part of the LIN frame (Synch field, data and CRC).

This prescaler modification is only used for the application development using the emulator.

The final ST92F250 application uses just one prescaler and sets the LINE bit in the SCI-A initialization code.

2.3 SECOND I2C

The I2C-1 cannot be emulated but the code validation can be done as a separate application using the I2C-0.

When the I2C-1 is being used, external addresses A[18:17] are no longer available. This is not the case with the ST92F150 emulator as the second I2C is not available. Take care not to use these addresses.

2.4 EXTERNAL MEMORY ACCESS

The external memory access should be emulated with EMR1.BSZ bit=0.

This will configure the P4[7:6]-P6[5:4] signals in Standard mode. If High Drive mode is needed for the I2C communication (with EMR1.BSZ bit=1), it should be emulated separately from the external memory access (with EMR1.BSZ bit=0).

2.5 P3.0, P6.6 AND P6.7

These general purpose I/Os cannot be emulated.

2.6 TOOLCHAIN INCLUDE FILES

All the ST92F250 features are described in the STVD9 V6 ToolChain include files.

Use the following statement:

```
#include <sys\st92f250\st92f250.h>
#include <sys\st92f250\flash.h>
#include <sys\st92f250\i2c0.h>
#include <sys\st92f250\i2c1.h>
```

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