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Web Server Reference Design Using a PowerPC-Based Embedded System

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Summary

This application note details an embedded system example design of a web server running on a PowerPC™ core within a Xilinx Virtex-II Pro™ FPGA. The system is designed using the Embedded Development Kit (EDK). The application note also explains how to set up a system as a web client and how to connect to the web server running on the PowerPC processor.

Hardware Requirements

- Memec XC2VP4 Development Board (Rev. 1) with P160 Communications module.

  The development board contains a Xilinx XC2VP4 Virtex-II Pro™ FPGA.

  See "Porting the Design to Memec XC2VP4 Rev. 2, Rev. 3, or Rev. 4" for information on porting this design to later revisions of the Memec XC2VP4 Development Board.
- JTAG Parallel 4 Cable
- Cross-over Ethernet Cable

Software Requirements

- Embedded Development Kit (EDK) 6.3.
- ISE 6.3i.
- Internet Explorer, Netscape, or Mozilla web browser.
- Web server EDK project (downloaded from Xilinx web site). The project can be opened in the Xilinx Platform Studio (XPS), through which the web server design can be customized and downloaded to the Xilinx FPGA.

  The PowerPC server design can be downloaded from:

  http://www.xilinx.com/ise/embedded/memec_v2p.zip

Introduction

The embedded system design used in this application note contains these components (see Figure 1):

- A PowerPC processor connected to 32 KB of BRAM memory over the Processor Local Bus (PLB).
- A UARTLite, an external SRAM memory interface, an Ethernet 10/100 MAC, and a General Purpose I/O (GPIO), all connected to the On-chip Peripheral Bus (OPB) through a PLB2OPB Bridge.

All of the IP cores used in the design are described in the *Processor IP Reference Guide* included with the EDK.

In the design, four GPIO output bits are connected to LEDs LED1 – LED4 on the development board and four input GPIO bits are connected to DIP switches DIP1 – DIP4. In the design example, the Ethernet MAC is running at 100 Mb/s. To run the example the peer network connection needs to be set to 100 Mb/s.

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Note: The 10/100 Ethernet MAC PLB peripheral (PLB_ETHERNET) used with this design is not a free core. To use the core an evaluation license is required; the evaluation license is included with the EDK. The evaluation version of the core includes built-in timeout circuitry which disables the core after a period of time.

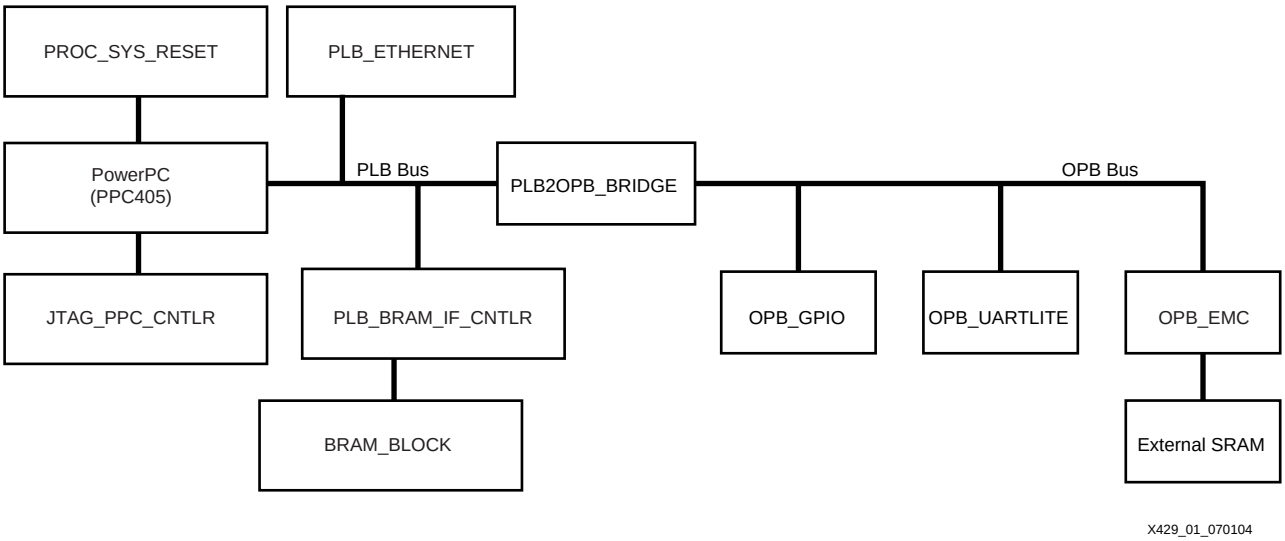

Figure 1: **PowerPC Web Server Design**

Table 1 shows the devices used in the web server design and the memory map for the design.

Table 1: **Web Server Design Devices**

Device	Hardware Version	Address		Size (Bytes)	Comment
		MIN	MAX		
PPC405	2.00.c	N/A	N/A	N/A	PowerPC Processor
BRAM_BLOCK	1.00.a	N/A	N/A	N/A	Block RAM
PLB_BRAM_IF_CNTLR	1.00.b	0xFFFF_8000	0xFFFF_FFFF	32k	Memory controller for block RAM
PLB_ETHERNET	1.01.a	0x6000_0000	0x6000_3FFF	16k	Ethernet MAC
OPB_GPIO	1.00.a	0x80EF_0100	0x80EF_01FF	256	DIP switch input, LED output
OPB_UARTLITE	1.00.b	0x80EF_0200	0x80EF_02FF	256	Serial I/O
OPB_EMC	1.10.b	0x80D0_0000	0x80D0_00FF	256	External SRAM Memory Controller
JTAGPPC_CNTLR	1.00.b	N/A	N/A	N/A	Connects PowerPC debug port to FPGA JTAG chain
PROC_SYS_RESET	1.00.a	N/A	N/A	N/A	Processor System Reset Module

The Web Server

The web server source code is located in the project's `/code` directory. The LibXil networking and file system libraries accessed by the web server design are included by LibGen, the Library Generator utility. The layout of the program is controlled by the linker script `code/linker_script`. The program is running off the external SRAM memory.

On this system the web server is running HTTP 1.0. A file system, built using the LibXil Memory File System library, stores the files. The server listens for requests at port 8080. Every request is processed, then replies are served up by the server to the client.

Operations Performed by the Web Server

The web server in the design displays a web page (see Figure 2) through which these operations can be performed:

- HEX-digit LED Display

  When a HEX digit is typed in the web page, it is displayed as a four-digit binary number on the board's LEDs when the web page is reloaded.

- Changing Colors

  The background color changes each time the web page is reloaded.

- DIP Switches

  Set the board's DIP switches (DIP1, DIP2, DIP3, DIP4) and a binary value is displayed on the web page when the web page is reloaded.

Note: For details on how the web server software design works, see the Web Server Flowchart in Figure 4.

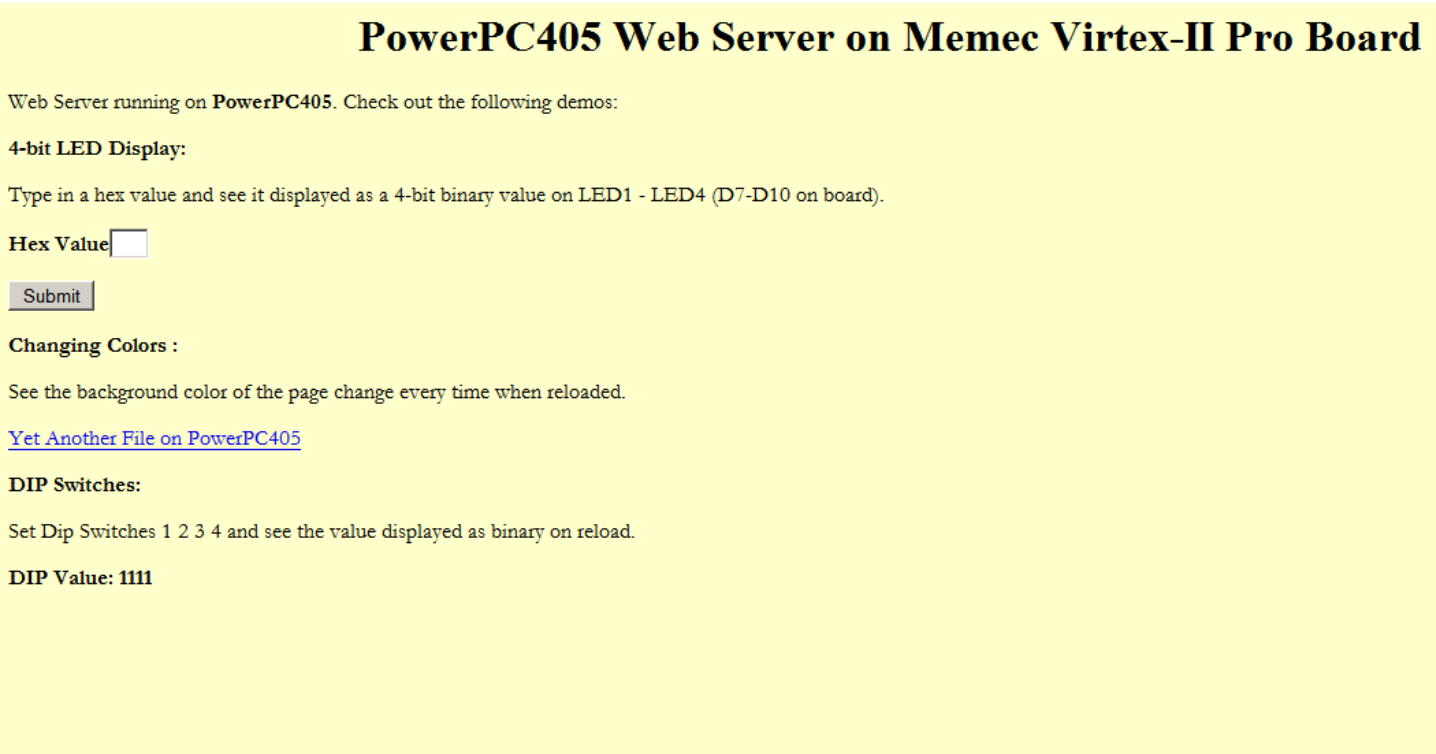

Figure 2: **Web Page to Control Web Server Operations**

Opening the Web Server Design

To open the web server project in the EDK:

1. Unzip the included design files.

   The design files are the EDK project files describing the web server.

2. Open the Xilinx Platform Studio (XPS) (**Start** → **Programs** → **Xilinx Embedded Development Kit** → **Xilinx Platform Studio**).
3. In XPS, select **File** → **Open Project**. The Open Project dialog box appears.
4. Browse to the `system.xmp` file in the `memec_v2p/PPC` directory, then open the `system.xmp` file in XPS.

Generating the Netlist and Implementing the Design

To generate the system netlist and implement the hardware design:

1. Generate the netlist by selecting **Tools** → **Generate Netlist** in XPS.

   Observe the progress of the operation in the XPS transcript window.

   The evaluation license for the 10/100 Ethernet MAC core is used to generate the netlist for that core.

2. Implement the design by selecting **Tools** → **Generate Bitstream** in XPS.

   Observe the progress of the operation in the XPS transcript window.

   When XPS implements the system, it accesses a UCF constraints file for the Memec XC2VP4 board. The UCF file is located in the supplied `/data` directory. XPS also uses the OPT option file included in the `/etc` directory.

Viewing the Libraries Used in the Design

The EDK contains software library support for networking and memory file systems. The web server design running on the PowerPC processor uses the XilNet networking library and the XilMfs memory file system library.

To view the library settings for the web server design:

1. In the System tab of the XPS project view window, double-click **System BSP** → **CPU PPC405_i**.
2. In the **Software Platform** tab of the Software Platform Settings dialog box, observe the **Libraries** table at the bottom left corner of the dialog box (see Figure 3).

   The table indicates that the Xilnet and XilMfs libraries are used in the design.

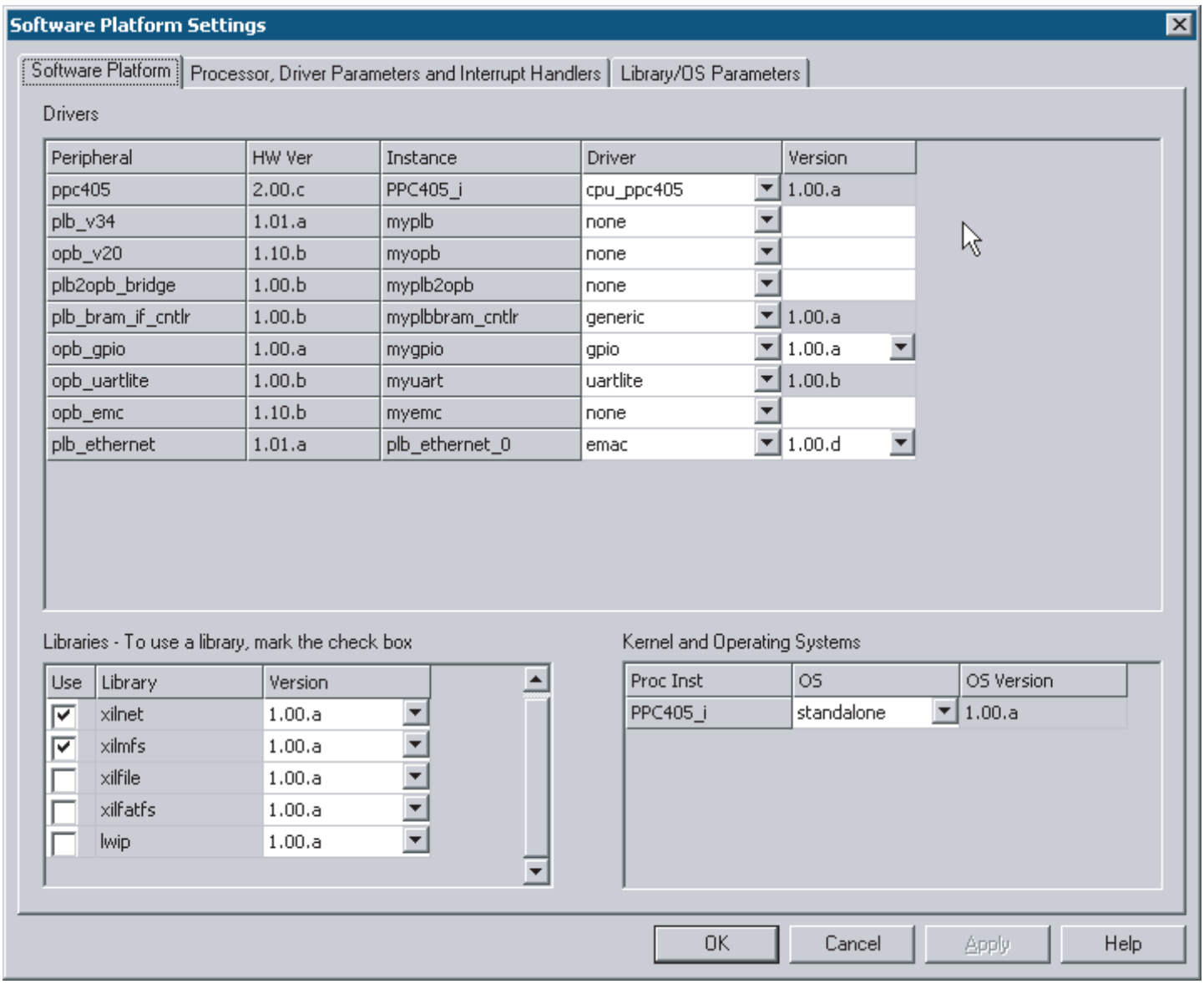

Figure 3: **Libraries Table in Software Platform Settings Dialog Box**

Configuring the Web Server and Compiling the Web Server Code

The Ethernet MAC requires IP and MAC addresses to be initialized and set in the web server code. In the demonstration EDK project, the IP address must be set for the web server to work properly.

To set the web server IP address:

1. In the XPS project view window, open the `web.c` source file by double-clicking **code/web.c**, located in the **Applications** tab, under **Project** → **Sources**.
2. Browse to the line `xilnet_ip_init("1.2.3.4");`.

   The line numbers of any open text documents are displayed on the lower right-hand side of XPS.
3. In the `xilnet_ip_init` function call, do one of the following:
   - Leave the argument set to `1.2.3.4` (which will require you to change your host's IP address)

OR

- Change the argument to match the local IP address of your host.

4. Save the changes to `web.c`.
5. Select **Tools** → **Build All User Applications** to compile the web server design.

Downloading the Web Server Code

Once the web server code is compiled, the download program must be updated and downloaded to the FPGA.

To download the code to the FPGA:

1. In XPS, select **Tools** → **Update Bitstream**.

   In the XPS transcript window, observe that the bitstream is updated by the iMPACT (ISE device configuration) tool.

   Note: The iMPACT GUI cannot be open when the **Update Bitstream** command runs.
2. Connect the JTAG Parallel 4 cable from the PC to the Memec XC2VP4 board.
3. In XPS, select **Tools** → **Download**.

   The bitstream is downloaded to the development board by the iMPACT tool.

   When the FPGA device is configured, the DONE light is illuminated on the development board.

Configuring the Web Client and Running the Web Server Demo

1. Unplug any Ethernet cable connected to the host PC and connect the crossover Ethernet cable to the PC and to the P160 Ethernet module.

   The JTAG Parallel 4 cable must also remain connected from the PC to the Memec XC2VP4 board.
2. Modify the host PC's IP address so it is in the same subnet as the web server. To change the PC's IP address:
   a. Select **Start** → **Settings** → **Control Panel** on the Windows desktop.
   b. Double-Click **Networking and Dialup**.
   c. Right-click the applicable LAN connection, then select **Properties**.
   d. Select **Internet Protocol** and click **Properties**.

Note: When the PC's IP address is changed in the following steps, note the original property settings, so the properties can be changed back after performing the demo.

   e. In the Internet Protocol Properties dialog box, select **Use the following IP Address**.
   f. In the **IP address** box, enter a unique IP address in the same subnet as the one specified for the web server. For example, if the IP address specified for the web server was 1.2.3.4, the IP address of **`1.2.3.9`** can be entered in the **IP Address** box.
   g. Click **OK** on the Internet Protocol Properties dialog box.
   h. If a message appears indicating that a subnet mask is missing, Select **OK**. Select **OK** again and again.
3. In XPS, select **Tools** → **XMD**. This will load the application code via the JTAG connection to the JTAGPPC controller using XMD. The XMD console should display `Web Server Running`.

Note: XMD (Xilinx Microprocessor Debugger) is the EDK debug engine for embedded systems. It includes a TCL environment which allows you to create fully customized debug tools. After launching XMD, it will source xmd.ini if the file is present in the EDK project directory. The xmd.ini file contains a list of TCL commands to run each time XMD runs.

4. Open an HTML browser and point to the URL **`http://`***x.x.x.x***`:8080`**, where *x.x.x.x* is the IP address you specified for the web server.

   Note: If the browser uses a proxy to access the Internet, disable the proxy setting and enable a direct connection to the Internet.

5. The web server demo page should appear in the browser (see Figure 2). Follow the instructions to read the DIP switch values and write to the LEDs on the development board.

   For details on how the web server software design works, see the Web Server Flowchart in Figure 4.

Porting the Design to Memec XC2VP4 Rev. 2, Rev. 3, or Rev. 4

To port the web server design to the newer Rev. 2, Rev. 3, or Rev. 4 boards, make these two changes:

- Part Change: (Only if Rev 2, 3 or 4 has an xc2vp7 FPGA). Change the part in XPS from xc2vp4 fg456 to xc2vp7 fg456.
- UCF File Change:

```
NET "ETH_RXD<2>"    LOC = "G20"; #LIOA15, Rev1
#NET "ETH_RXD<2>"    LOC = "F11";  #LIOA15, Rev2,3, or 4
```

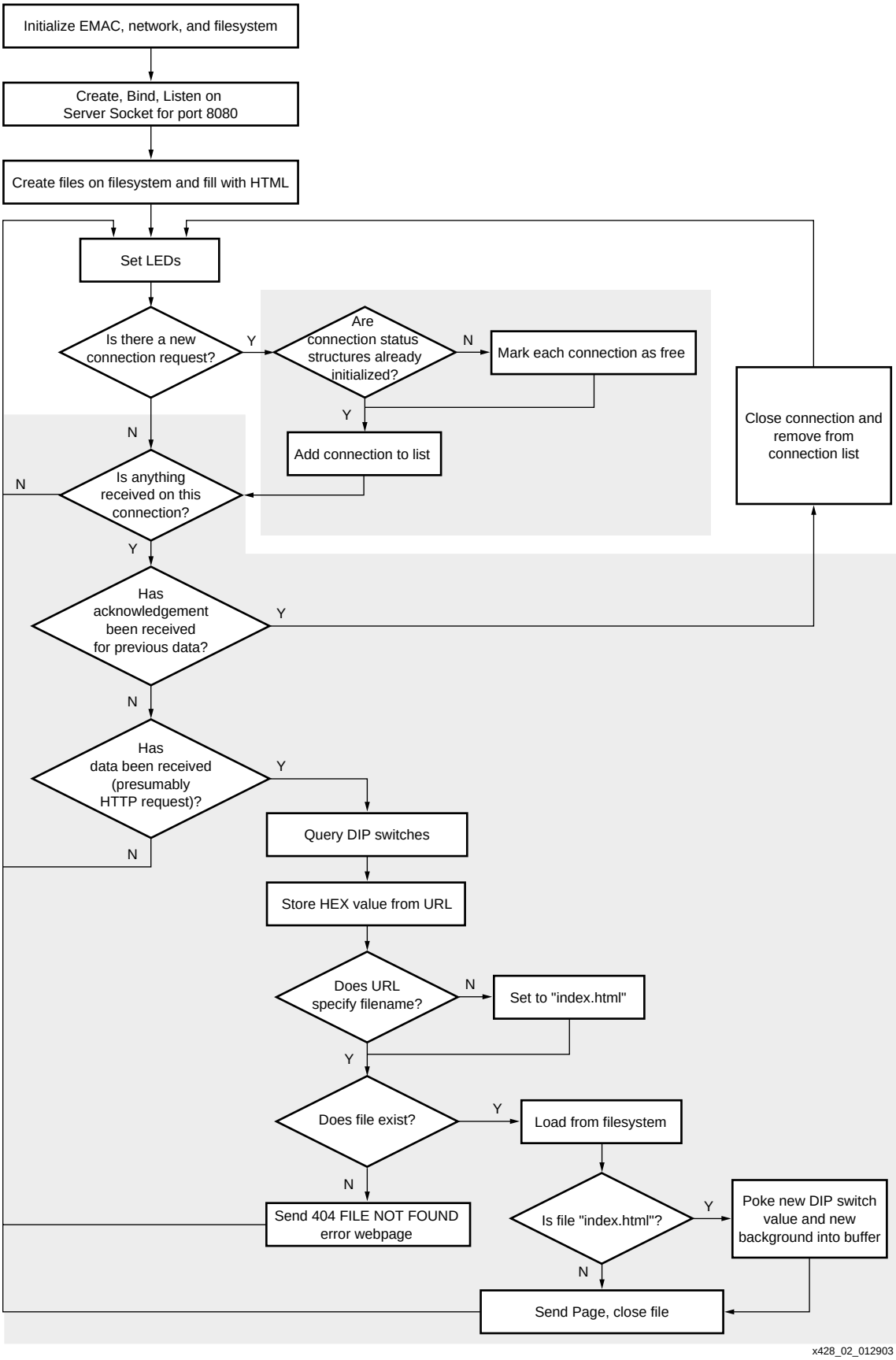

Figure 4: **Web Server Flowchart**

Reference Design

The PowerPC web server design files can be downloaded from:

http://www.xilinx.com/ise/embedded/memec_v2p.zip

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/30/04	1.0	Initial Xilinx release in Application Note template.
11/3/04	1.1	Revised for EDK 6.3i release.