Simulators shred the limits of mixed-signal design

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As process sizes continue to shrink, mixed-signal designers face a number of challenges that affect design closure. Shrinking feature sizes, finer line widths, longer interconnect and more routing layers make it possible to pack more functionality onto a chip. With the increase in functionality, these advanced mixed analog/digital SoC designs push the technology envelope with higher clock frequencies, lower power-supply voltages and increased power consumption. There is a big increase in noise sources in these designs; yet HF signals must run reliably in spite of it.

Deep-submicron mixed-signal designs experience performance deterioration, silicon failure and reliability problems because of a plethora of design integrity phenomena. Exhaustive analysis of these issues can no longer be done manually but must become part of the automated design flow. Also, with escalating mask costs, there is a crucial need for new post-layout analysis methods that uncover problems before a chip is manufactured.

Recognizing design issues

Analyzing a design for these problems can result in potentially conflicting data. Engineers must decide on the main design criteria and minimize related issues. But not all issues can be minimized. Since designers, up until now, lacked solutions such as full-chip parasitic extraction tools. They tried to avoid problems through overdesign–increasing timing margins, guardbanding, distancing analog and digital blocks and power and grounds, and increasing space between buses and nets.

These methods cannot solve the problems of nanometer designs, because of the enormity of design sizes and signal net counts. On-chip real estate is at a premium, and there are too many nets critical to the design to apply these overly conservative measures. Indeed, doing so may even cause new problems such as inductive-coupling effects.

Signal-integrity issues such as crosstalk, substrate noise, IR drop, electromigration and power dissipation have unique effects on a design. Now with the migration toward new processes, traditional tools are being found wanting.

Crosstalk: In the case of crosstalk, for example, getting overly conservative by spacing wires too far apart can affect the area budget and necessitate the move to a bigger, and more expensive, package.

However, traditional parasitic-extraction and analysis solutions lack the capacity and technology to process nanometer full-chip designs at transistor-level accuracy. Detailed analysis of crosstalk noise requires accurate, full-chip transistor-level parasitic extraction that includes cross-coupling capacitors. But this results in extremely large netlists because of the amount of parasitic elements included. A high-capacity, full-chip mixed-level simulator is needed to process these netlists and account accurately for the hierarchical interactions between the analog and digital boundaries.

Substrate noise: This is becoming an important issue for mixed-signal SoC design. Whenever digital signals switch, current is injected into the substrate via capacitive coupling of the devices, wells and interconnect. This noise is propagated into the analog circuits, which are very noise-sensitive (**Figure 1**). Thus, the analog circuitry's performance can be crippled or it can fail entirely.

Various design guidelines for minimizing substrate noise have been proposed. They include trench isolation of analog devices from the substrate region and the use of guard rings to surround digital circuitry known to inject large substrate currents. The location of noisy digital and sensitive analog blocks as far apart as possible is another popular method.

However, these design techniques can be costly in terms of area budget, and they cannot be applied to HF designs, where there is no possibility to lower clock frequencies. Therefore, analysis of substrate-coupling effects is becoming more critical for high-speed nanometer applications. But it is not sufficient to merely analyze the substrate parasitics. The substrate parasitic network has to be extracted together with the interconnect parasitic network to get an accurate account of the signal coupling through the substrate. An efficient simulation solution is needed to guarantee the optimum isolation by minimizing design area and considering dominant noise frequency components.

IR drop: At around the 130nm node, power-supply voltage or IR (current, resistance) drop becomes increasingly significant. Increased losses are compounded by lower supply voltages. In addition, power-supply voltage drop affects circuit performance by increasing overall delay and reducing noise mar-

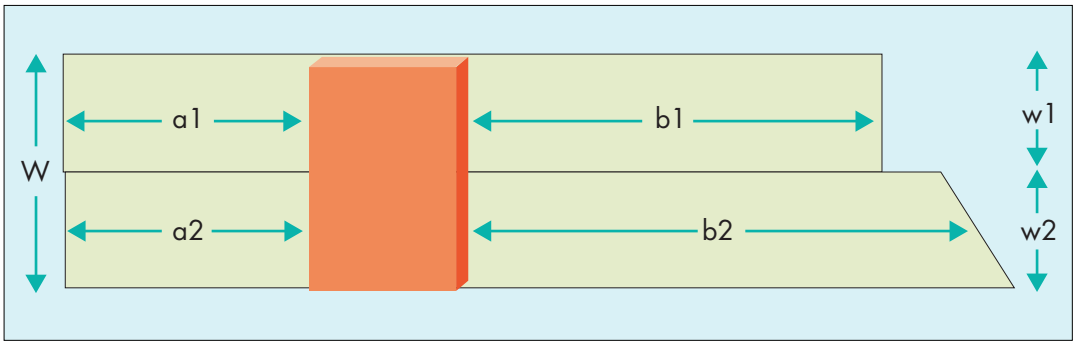

Figure 2: Irregularly-shaped diffusion is not recognized in simulation unless exact measurement is taken of all physical parameters.

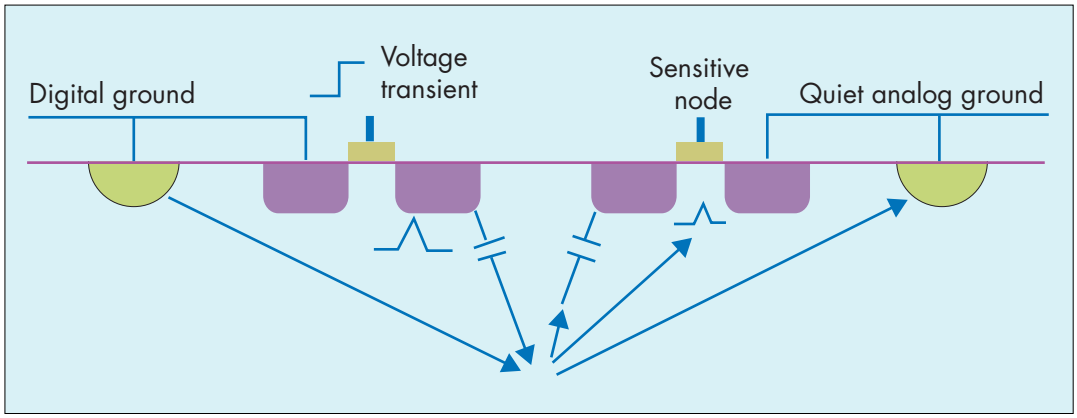

Figure 1: The substrate region can be a major propagation path for coupling noise between digital and analog blocks. High-speed circuits are particularly sensitive, with the problem compounded by smaller geometries.

gin. In a 130nm design, IR drop can increase path delays by 50 percent.

In the past, static timing analysis methods were used to measure IR drop. These methods were fast but inaccurate, since they missed transient problems such as simultaneous switching and inductance effects. Other simulation approaches shoot for increased accuracy but cannot handle full-chip designs in one shot. Such methods also prove insufficient since they miss on-chip interactions and affect turnaround time. Accurate IR drop analysis must consider the power grid and the entire circuit simultaneously. A fast, transistor-level dynamic analysis tool is required that can handle today's large design sizes and can analyze the transient as well as static components of power and signal net voltage drop.

Electromigration: The problem of electromigration stems from the dislocation and transport of atoms in a metal line along the direction of current (electron) flow. High current density accelerates the process. Over time, electromigration can cause areas of breakage or buildup in wires, causing open- or short-circuits. Joule heating–the energy produced by the collision of electrons with the lattice–increases the temperature in the wires, which can also contribute to electromigration. To minimize the rate of electromigration, peak, average and rms current densities and temperatures of both power and signal nets need to be calculated.

For large mixed-signal designs, transistor-level SPICE-accurate tools are needed for capacity, speed and accuracy. On the process technology front, copper processes have been used to control electromigration. However, copper's effects on resistivity restricts its usage for very fine-pitch circuits.

Power consumption: Long a concern for low-power devices, power dissipation is increasing with smaller process geometries and increasing device count and density in nanometer designs. There are three main sources of power dissipation in CMOS chips: dynamic charging (or switching power), leakage current and short-circuit current. Switching power accounts for the majority of the operating power in a device, though leakage and short-circuit power are major concerns for nanometer designs as well.

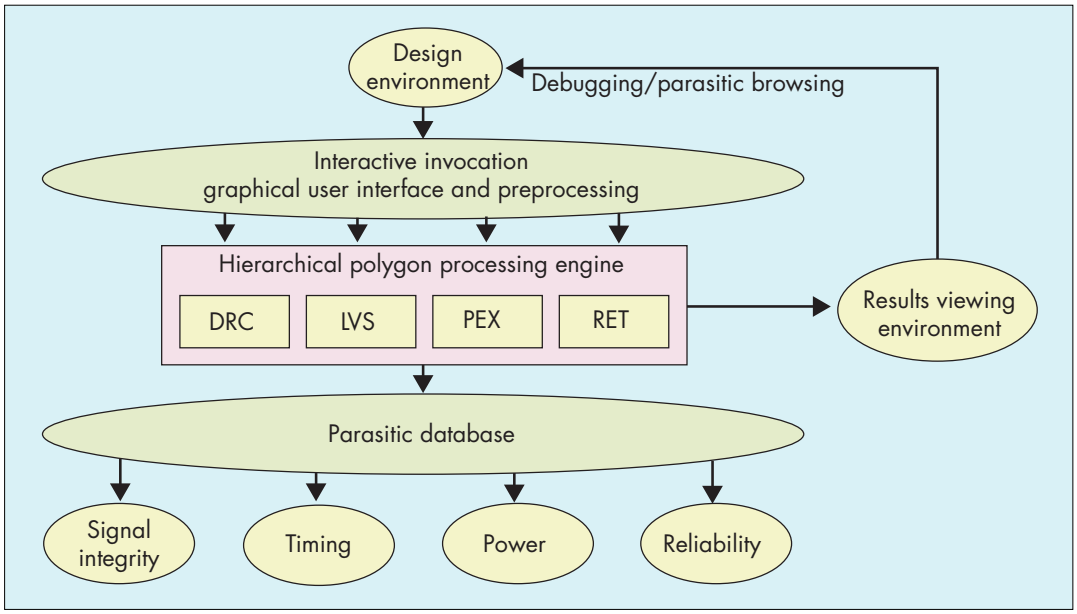

Figure 3: The right recipe of tools comprises an accurate design-closure methodology with hierarchical LVS and mixed-level parasitic extraction with coupling accuracy, followed by full-chip, high-speed post-layout analysis.

During design, areas of high power dissipation need to be identified. Fixes include adjusting transistor threshold voltages and controlling the switching power with multiple voltage domains. Traditional analysis tools are lagging in the ability to handle multimillion-transistor designs with transistor-level accuracy and speed. Designers now need an accurate, high-speed, high-capacity circuit simulator that calculates average, rms, peak and instantaneous currents down to the transistor level. Both static and dynamic analyses are necessary to identify short-circuit currents, leakage currents and charging currents.

A new approach

Given that more than 80 percent of designs are failing first silicon (Collett International, "2001 IC/ASIC Design Closure Study"), designers of analog and mixed-signal SoCs are in urgent need of new, accurate post-layout analysis solutions. This methodology must include a parasitic-extraction tool that offers a comprehensive, accurate, hierarchical transistor-level approach. It must include the highest possible extraction accuracy coupled with increased performance, integration to a layout-vs.-schematic (LVS) netlist comparator and the ability to integrate with analog/mixed-signal design environments.

Extraction accuracy: In mixed-signal designs, accurate parasitic extraction is the key to accurate and comprehensive analysis. To achieve this analysis level, designers need a solution that is flexible in precisely extracting critical nets while simultaneously extracting the full design. This ensures accuracy by accounting for all critical coupling and inductive effects between signal nets and to power nets.

Traditional paths to maximizing extraction accuracy have resulted in large, complex netlists and hierarchy destruction, thereby crippling SPICE simulators. To address this problem, hierarchy in the post-parasitic netlists needs to be preserved as much as possible. Hierarchical, transistor-level extraction and simulation can improve the capacity, accuracy and speed requirements for nanometer advanced mixed-signal SoC.

In a hierarchical netlisting flow, the user can define the extraction accuracy level, be it gate or transistor level, for all the lower-level cells in the design hierarchy. The hierarchical cells can reside at any level in the hierarchy. The resulting mixed-level netlist reflects the needed hierarchy with transistor accuracy for all critical blocks and gate-level accuracy for digital and noncritical cells. It is as compact as possible for efficient downstream simulation without sacrificing accuracy.

Integration to LVS: Accurate extraction of layout devices and their physical parameters is required for any intentional advanced mixed analog/digital circuit component. Analog designs often contain specific devices such as inductors, varactors and variable resistors. An LVS tool needs to extract these devices and precisely measure their special physical parameters. Those properties are compared with the model properties in the source netlist and can be required to meet a user-defined tolerance. Precision is the key here: Sensitive analog components have minuscule tolerances. To close the loop from simulation, physical design and extraction back to simulation, the LVS tool also has the task of back-annotating the source netlist device and net names onto the extracted layout netlist. This enables the designer to use the prelayout simulation stimulus files for postlayout simulation.

In addition, design-for-manufacturability issues at 90nm process technology will require an even stronger coupling between LVS and parasitic extraction. With 90nm now making its debut, nonstandard elements such as handcrafted analog components or MOS devices with irregularly shaped diffusion regions have less wiggle room and therefore are more

susceptible to current-related issues. The only way to accurately assess the stress effect of these components is through post-layout resimulation, with both parasitic effects and new, accurately measured physical device parameters (**Figure 2**). Without a tight link between an LVS tool, which can extract these new device parameters, and an accurate parasitic-extraction tool, this cannot be properly netlisted for resimulation purposes.

Integration with analog/mixed-signal design: An integrated debug and repair loop between analysis and design tools is critical for design closure. An interactive verification interface facilitates interoperability among tools and completes the integration among simulation, verification and analysis through efficient data handling from and to analog and full-custom design environments, extraction and post-layout analysis. Through an interactive GUI, the designer can set and execute all components of the mixed-signal post-layout analysis flow.

Designers need to be able to back-annotate to and browse parasitic-extraction results in the design environment, such as selecting an individual net and viewing the associated parasitic capacitance and resistance. An efficient results-viewing and -debugging environment can greatly enhance the post-layout analysis cycle. Another benefit of integrated post-layout analysis is the capability of selectively annotating parasitics to the various blocks in the design. Since only the block's parasitics are added to the netlist, the result is a smaller simulation netlist and therefore faster results. It's a way to determine what effects a single block's parasitics have on the overall circuit design.

With the right recipe of tools, designers will possess an accurate design-closure methodology consisting of hierarchical LVS and hierarchical mixed-level parasitic extraction with coupling accuracy, followed by full-chip, high-speed post-layout analysis. Actual parasitic effects are included, with transistor-level accuracy where it is needed. With this combination of attributes, prelayout hierarchy is preserved in post-layout, enabling fast execution (**Figure 3**). □

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