Intel StrataFlash® Memory to Intel® IXP42X Product Line of Network Processors and Intel® IXC1100 Control Plane Processor Design Guide

Application Note 785

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Revision History

Date of Revision	Version	Description
August 03	-001	Initial Release
September 04	-002	The following figures and tables were updated: Figure 1. Processor System Block Diagram Table 5. Expansion Bus Configuration Register 0 Table 6. Expansion Bus Bit Level Description of the Configuration Register 0

1.0 Introduction

This application note covers the interface between the following:

- Intel StrataFlash® Memory Device (called hereafter the J3 Flash Memory Device)
- Intel® IXP42X Network Processor (called hereafter the IXP42X Processor) and Intel® IXC1100 Control Plane Processor (called hereafter the IXC1100 Processor)

This application note also discusses general concepts involved when interfacing the features and control signals of the J3 flash memory device.

This document was written based on information available at the time for the J3 Flash Memory Device and the Intel® IXP42X product line and IXC1100 control plane processors. Any changes in specifications to either device may not be reflected in this document. Refer to the appropriate documents or sales personnel for the most current information before finalizing any design.

2.0 Intel StrataFlash® Memory Device

The J3 Flash Memory Device provides 2x the bits in 1x the space compared to previous generation devices. It is available in 32-, 64-, and 128-Mbit densities. The J3 Flash Memory Device provides two-bit-per-cell storage technology. Features include asynchronous page-mode reads, buffered writes, and individual block locking.

Other benefits include support for code and data storage. The J3 Flash Memory Device is ideal for applications where high density and low cost are required. Examples include networking, wireless communication devices, storage applications, telecommunications, digital set-top boxes, audio recording, and digital imaging.

3.0 Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor

The IXP42X Processor and IXC1100 Processor contain an Intel® StrongARM* V5TE architecture compliant microprocessor referred to as Intel XScale® technology. The processor has been designed for high performance and low power. It leads the industry in mW/MIPs performance.

The IXP42X Processor and IXC1100 Processor are designed with Intel® 0.18-µ production semiconductor process technology. This process technology, along with the compactness of the Intel® StrongARM* RISC ISA, simultaneous processing of three integrated network processing engines, and numerous dedicated function peripheral interfaces enables the IXP42X Processor and IXC1100 Processor to operate over a wide range of low-cost networking applications, producing industry-leading performance.

IXP42X Processor and IXC1100 Processor provide:

- Two MII interfaces
- Intel® IXB8055 UTOPIA/POS Reference Design level 2 interface
- A USB v1.1 device controller with embedded transceiver
- A 32-bit, 33-MHz/66-MHz PCI bus
- A 32-bit, 133-MHz SDRAM interface
- Two Universal Asynchronous Receiver/Transmitters (UARTs)
- Two high-speed serial interfaces
- 16 General Purpose Input/Output interfaces (GPIOs) and a 16-bit expansion bus

The Expansion Bus Controller provides an interface from internal South Advanced High Performance Bus (AHB) to external flash, Host-Port Interfaces (HPI), and other slow-speed devices.

4.0 Hardware Interface

This section describes the hardware interface signals between the J3 flash memory device, the IXP42X Processor, and IXC1100 Processor. This document assumes that all other device signals and power supplies are connected in such a way as to ensure proper device operation.

4.1 Flash Memory Interface

Table 1 lists the J3 Flash Memory Device hardware Interface signals:

Table 1. J3 Flash Memory Device Hardware Interface Signals

J3 Flash Memory Device Signal	Description
A0 BYTE ADDRESS	Device byte address input. A0 is the least significant byte (x8) address line; A0 is not used in x16 mode (BYTE#-high).
A[23:1] ADDRESS	Device address inputs. A1 is the least significant word (x16) address line.
D[7:0] LOW-BYTE DATA BUS I/O	Inputs during write operations, outputs during read operations, and High-Z (float) when the device is deselected, or OE# deasserted.
D[15:8] HIGH-BYTE DATA BUS I/O	Inputs during write operations, outputs during read operations, and High-Z (float) when the device is deselected or OE# deasserted.
CE[2:0] CHIP ENABLE	Active low input. Activates the J3 Flash memory Device's control logic, input buffers, decoders and sense amplifiers. When the J3 Flash memory Device is deselected, power is reduced to standby levels.
OE# OUTPUT ENABLE	Active low input. OE#-low enables the output buffers. OE#-high disables the output buffers and places all the data outputs at High-Z.
WE# WRITE ENABLE	Active low input. WE#-low enables the write buffers. Input data is latched on the rising edge of WE#. WE#-high disables the write buffers.
VPEN PROGRAM/ERASE ENABLE	Input. The voltage applied to VPEN must be greater than VPENLK to program or erase array blocks or to configure block lock bits.
RP# RESET/POWERDOWN	Active low input. RP#-low resets internal automation and inhibits write operations. RP#-high enables normal operation. Exit from reset sets the J3 Flash memory Device in read array mode.
STS STATUS	Open-drain output. Indicates status of the internal state machine. (Not used in this example design.)
BYTE# BYTE ENABLE	Active-low input. BYTE#-low places the J3 Flash memory Device in x8 mode. Data is input and output on DQ[7:0] only; DQ[15:8] float (High-Z). Address bit A0 is active and is the least-significant byte (x8) address line. BYTE#- high places the J3 Flash memory Device in x16 mode. The A0 input buffer is turned off, and A1 becomes the least significant work (x16) address line. DQ[15:0] is used for input and output.

4.2 Processor Memory Interfaces

The IXP42X Processor and IXC1100 Processor contain an Expansion Bus Controller to interface to a variety of components that do not have PCI bus interfaces or do not optimally reside on the PCI Bus. Examples of such components include flash memory, SRAM memory, simple displays, Digital Signal Processors (DSPs) with host interface ports, Digital/Analog converters, programmable logic, and control interfaces to devices such as UTOPIA or other PHY components. See Figure 1, “Processor System Block Diagram.

Figure 1. Processor System Block Diagram

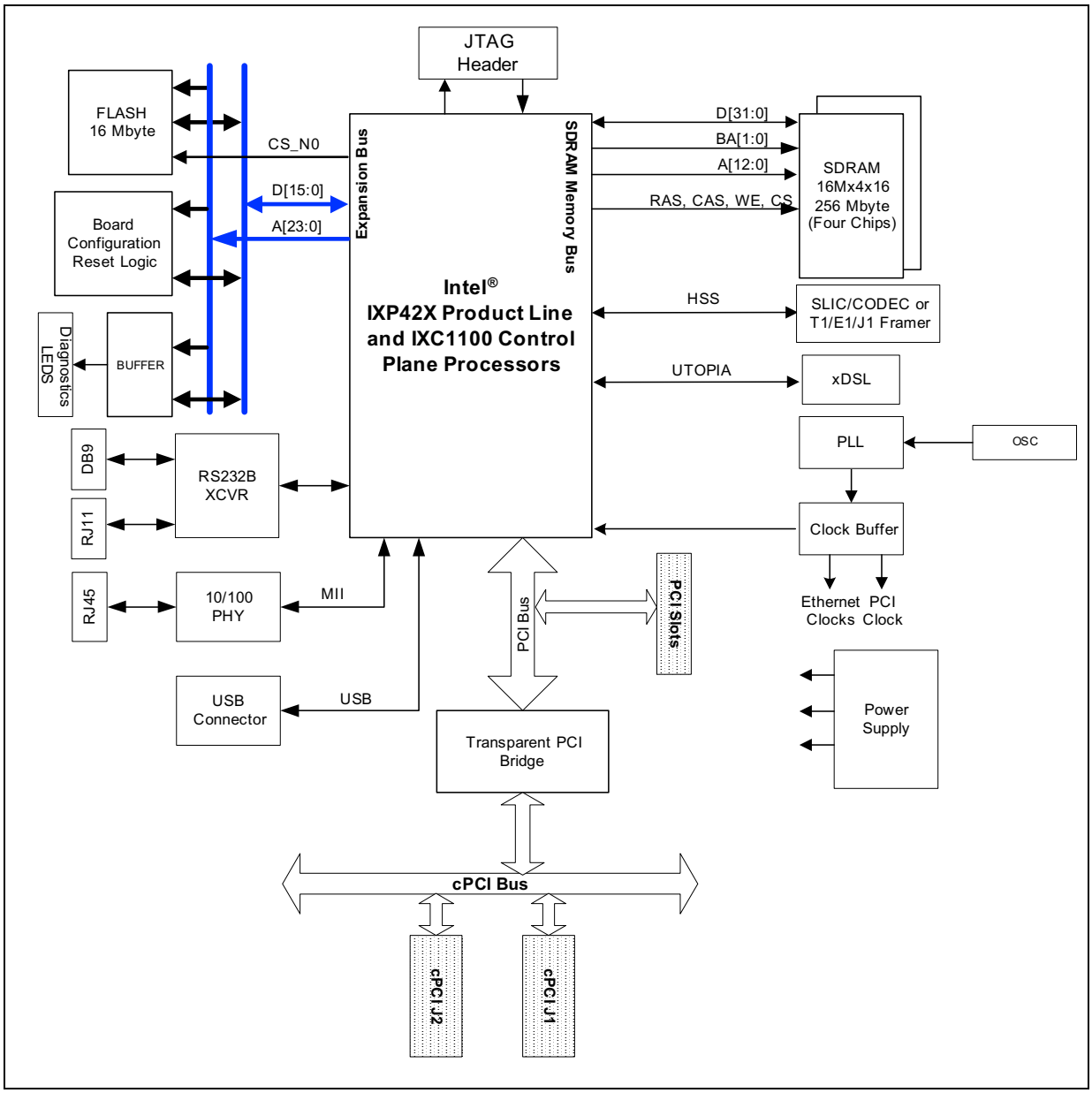


Table 2 describes the J3 Flash Memory Device expansion bus interface signals:

Table 2. J3 Flash Memory Interface Signals for the Expansion Bus

J3 Flash Memory Interface Signal	Description
EX_ADDR[23:0]	Expansion Memory Address Bus (output): Provides the address used for memory accesses.
EX_DQ[15:0] Expansion Data Bus (I/O)	Inputs during read operations: outputs during write operations.
EX_WR_N Write Strobe (output)	Intel mode write strobe / Motorola mode data strobe / TI mode data strobe.
EX_RD_N Read Strobe (output)	Intel mode read strobe / Motorola mode read-not-write strobe / TI mode data strobe.
EX_CS_N[0] Static Memory Chip Select (output)	Flash memory chip select for expansion bus.
RESET_IN_N Reset (input)	Used as a reset input to the device after power up conditions have been met.

4.3 Interface Considerations

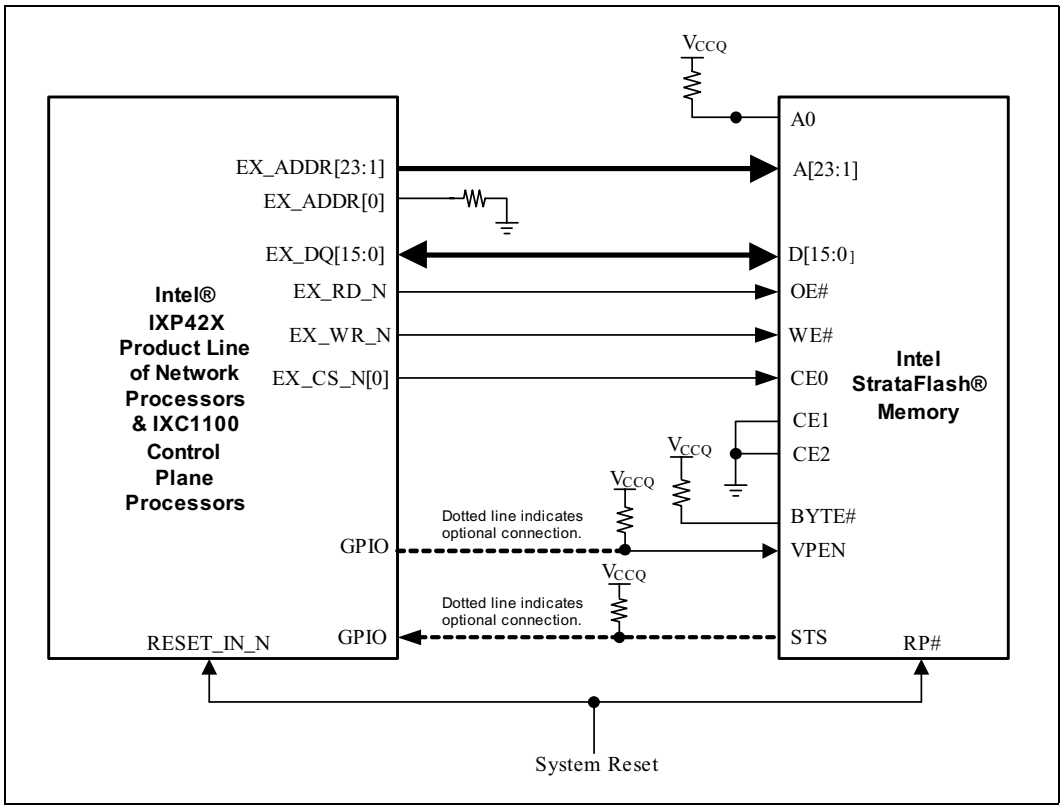
This design example uses one 128-Mbit device. The J3 Flash Memory Device interfaced with the Intel® IXP42X product line and IXC1100 control plane processors in a x16 data bus configuration. The expansion bus timing shown in this application note is running at 33 MHz. Other bus speeds and memory sizes can be implemented by modifying the design.

This sample interface does not include information regarding system initialization, interrupt control, exception handling, or other peripheral device operations. The signals/pins of external devices should be asserted or negated as necessary for desired device operation. Be sure to read all applicable documentation, such as datasheets, user's manuals, and errata before attempting to design with this interface. See Appendix A, “Additional Information” on page 18.

4.4 Hardware Considerations

Figure 2 shows the J3 Flash Memory Device connected to the IXP42X Processor and IXC1100 Processor. The BootROM address space supports up to 16-Mbyte (128-Mbit) of flash. The BootROM is mapped to the Intel XScale® core physical address 0x00. At start-up (reset), the IXP42X Processor and IXC1100 Processor begins fetching and executing instructions from address 0x00.

Figure 2. Block Diagram



5.0 Register Settings

After a system reset, the processor registers assume default values. The following sections describe the affected registers and their settings.

5.1 Flash Register Settings

There are no register settings to be configured on the J3 Flash Memory Device.

5.2 Processor Register Settings

The expansion bus controller registers are used to configure the operation of the external memory interface. The settings for the Timing and Control Register (EXP_TIMING_CS0) and the Configuration Register 0 (EXP_CNFG0) affect the interface timings for external memory accesses. These registers are described in the following sections.

Note: For current information, see the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processors Specification Update* and *Intel® IXP42X Product Line and IXC1100 Control Plane Processors Developer's Manual.*

Only the register bit fields that affect memory interface operations with the J3 Flash Memory Device are discussed. All other bit fields should be programmed as necessary to ensure proper operation.

5.3 Timing and Control Register

Each chip select on the expansion bus has a Timing and Control Register. In this design example, the boot device, a J3 Flash Memory Device, is connected to Chip Select 0 (CS0):

- Bit 31 of the Timing and Control Register (EXP_TIMING_CS0) enables or disables the flash memory device.
- Bits [29:16] of the EXP_TIMING_CS0 configure read/write flash memory accesses.

For this design example, configure EXP_TIMING_CS0 [31;29:16;6;4:3;1:0] with the following, assuming that the expansion bus is running at 33MHz in this example (and not 66MHz):

- EXP_TIMING_CS0 (CSx_EN [31]) = 1 (Chip Select x enabled)
- EXP_TIMING_CS0 (T1 - Addressing Timing [29:28]) = 01 (Extend address phase: 30ns)
- EXP_TIMING_CS0 (T2 - Setup / Chip Select Timing [27:26])= 01 (Extend setup phase: 30ns)
- EXP_TIMING_CS0 (T3 - Strobe Timing [25:22]) = 0100 (Extend strobe phase: 120ns)
- EXP_TIMING_CS0 (T4 - Hold Timing [21:20]) = 01 (Extend hold phase: 30ns)
- EXP_TIMING_CS0 (T5 - Recovery Timing [19:16]) = 01 (Extend recovery phase: 30ns)
- EXP_TIMING_CS0 (BYTE_RD16 [6]) = 0 (Byte access disabled)
- EXP_TIMING_CS0 (MUX_EN [4]) = 0 (Separate address and data buses)
- EXP_TIMING_CS0 (SPLT_EN [3]) = 1 (AHB split transfers enabled)
- EXP_TIMING_CS0 (WR_EN [1]) = 0 (Writes to CS region are disabled)
- EXP_TIMING_CS0 (BYTE_EN [0]) = 0 (= Expansion bus uses 16-bit-wide data bus)

Table 3, "Timing and Control Register for Chip Select 0" on page 12 describes the Timing and Control register of CS0. Table 4, "Bit Level Definition for each of the Timing and Control Registers" on page 12 describes the bit level description of the Timing and Control register.

Table 3. Timing and Control Register for Chip Select 0

Register Name:	EXP_TIMING_CS0																					
Hex Offset Address:	0XC4000000									Reset Hex Value:		0xBFFF3C4x										
Register Description:	Timing and Control Registers																					
Access: Read/Write																						
31	30	29	28	27	26	25... 22		21	20	19... 16		15	14	13... 10		9. 7	6	5	4	3	2	1	0
CSx_EN	(Rsvd)	T1		T2		T3		T4		T5		CYCLE_ TYPE		CNFG[3:0]		(Rsvd)	BYTE_RD16	HRDY_POL	MUX_EN	SPLT_EN	(Rsvd)	WR_EN	BYTE_EN

Table 4. Bit Level Definition for each of the Timing and Control Registers (Sheet 1 of 2)

Bits	Name	Description
31	CSx_EN	0 = Chip Select x disabled 1 = Chip Select x enabled
30		(Reserved)
29:28	T1 – Address timing	00 = Generate normal address phase timing 01 - 11 = Extend address phase by 1 - 3 clocks
27:26	T2 – Setup / Chip Select Timing	00 = Generate normal setup phase timing 01 - 11 = Extend setup phase by 1 - 3 clocks
25:22	T3 – Strobe Timing	0000 = Generate normal strobe phase timing 0001-1111 = Extend strobe phase by 1 - 15 clocks
21:20	T4 – Hold Timing	00 = Generate normal hold phase timing 01 - 11 = Extend hold phase by 1 - 3 clocks
19:16	T5 – Recovery Timing	0000 = Generate normal recovery phase timing 0001-1111 = Extend recovery phase by 1 - 15 clocks
15:14	CYC_TYPE	00 = Configures the expansion bus for Intel cycles. 01 = Configures the expansion bus for Motorola* cycles. 10 = Configures the expansion bus for HPI cycles. (HPI is reserved for chip selects [7:4] only) 11 = Reserved
13:10	CNFG[3:0]	Device Configuration Size. Calculated using the formula: SIZE OF ADDR SPACE = $2^{(9+CNFG[3:0])}$ For Example: 0000 = Address space of 2^9 = 512 Bytes … 1000 = Address space of 2^{17} = 128 Kbytes … 1111 = Address space of 2^{24} = 16 Mbytes
9:7		(Reserved)

Table 4. Bit Level Definition for each of the Timing and Control Registers (Sheet 2 of 2)

Bits	Name	Description
6	BYTE_RD16	Byte read access to Half Word device 0 = Byte access disabled. 1 = Byte access enabled.
5	HRDY_POL	HPI HRDY polarity (reserved for exp_cs_n[7:4] only) 0 = Polarity low true. 1 = Polarity high true.
4	MUX_EN	0 = Separate address and data buses. 1 = Multiplexed address / data on data bus.
3	SPLT_EN	0 = AHB split transfers disabled. 1 = AHB split transfers enabled.
2		(Reserved)
1	WR_EN	0 = Writes to CS region are disabled. 1 = Writes to CS region are enabled.
0	BYTE_EN	0 = Expansion bus uses 16-bit-wide data bus. 1 = Expansion bus uses only 8-bit data bus.

5.4 Configuration Register 0

The general-purpose Configuration Register 0 (EX_CNFG0) of the expansion bus is loaded at reset from the pull-ups or pull-downs on the expansion bus corresponding address lines. See the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processors Developer's Manual.* Bit 0 of the EX_CNFG0 configures the data bus width of the flash memory device. For this design example, configure EX_CNFG0 [0] with the following:

- EX_CNFGO (0) = 0. This configures the flash data bus width to 16-bits.

Table 5, "Expansion Bus Configuration Register 0" on page 13 defines the Configuration Register 0, and Table 6, "Expansion Bus Configuration Register 0 Description" on page 14 lists the pin-level description for Configuration Register 0.

Note: At system reset, once the boot sequence completes, bit 31 is written to a "0". This switches the default system memory map to place the SDRAM controller at address 0x00000000 to 0x0FFFFFFFF.

Table 5. Expansion Bus Configuration Register 0

Register Name:	**EXP_CNFG0**					
Hex Offset Address:	0XC4000020		**Reset Hex Value:**	0x8XXXXXXX		
Register Description:	Configuration Register #0					
Access: Read/Write.						

31	30						24	23	22	21	20			17	16											5	4	3	2	1	0
MEM_MAP	(Reserved)							CLK bit 2	CLK Bit 1	CLK Bit 0	User-configurable				(Reserved)												PCI_CLK	RES	PCI_ARB	PCI_HOST	8/16

Table 6. Expansion Bus Configuration Register 0 Description

Bit	Name	Description
31	MEM_MAP	Location of EXPBus in memory map space: 0 = Located at “50000000” (normal mode) 1 = Located at “00000000” (boot mode)
30:24		(Reserved)
23:21	Intel XScale core Clock Set[2:0]	Allow a slower Intel XScale core clock speed to override device fuse settings. However cannot be used to over clock core speed. Refer to Section 124, “Setting The Intel XScale® Core Operation Speed” on page 324 in *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer’s Manual* for additional details.
20:17		User-configurable. See the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer’s Manual* for additional comments.
16:6		(Reserved)
5		(Reserved)
4	PCI_CLK	Sets the clock speed of the PCI Interface 0 = 33 MHz 1 = 66 MHz
3	—	(Reserved)
2	PCI_ARB	Enables the PCI Controller Arbiter 0 = PCI arbiter disabled 1 = PCI arbiter enabled
1	PCI_HOST	Configures the PCI Controller as PCI Bus Host 0 = PCI as non-host 1 = PCI as host
0	8/16 FLASH	Specifies the data bus width of the flash memory device 0 = 16-bit data bus 1 = 8-bit data bus

6.0 Bus Operation and Timings

For the following discussion on bus operations and timings, refer to Table 7, "Read Timing Definitions" on page 15 and Table 8, "Write Timing Definitions" on page 15 for a description of all the flash memory timings shown in the waveforms. For a description of all processor timings, refer to the following tables:

- Table 3, "Timing and Control Register for Chip Select 0" on page 12
- Table 4, "Bit Level Definition for each of the Timing and Control Registers" on page 12
- Table 5, "Expansion Bus Configuration Register 0" on page 13
- Table 6, "Expansion Bus Configuration Register 0 Description" on page 14

Table 7. Read Timing Definitions

#	Symbol	Parameter Definition
R1	t_{AVAV}	Read/Write Cycle Time
R2	t_{AVQV}	Address to Output Delay
R3	t_{ELQV}	CEx to Output Delay
R5	t_{PHQV}	RP# High to Output Delay
R6	t_{ELQX}	CEx to Output in Low-Z
R7	t_{GLQX}	OE# to Output in Low Z
R8	t_{EHQZ}	CEx High to Output in High Z
R9	t_{GHQZ}	OE# High to Output in High Z
R10	t_{OH}	Output Hold from Address, CEx, or OE# Change, Whichever Occurs First
R16	t_{GLQV}	OE# to Array Output Delay

Table 8. Write Timing Definitions

#	Symbol	Parameter Definition
W1	t_{PHWL} (t_{PHEL})	RP# High Recovery to WE# (CEx) Going Low
W2	t_{ELWL} (t_{WLEL})	CEx (WE#) Low to WE# (CEx) Going Low
W3	t_{WP}	Write Pulse Width
W4	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CEx) Going High
W5	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CEx) Going High
W6	t_{WHEH}(t_{EHWH})	CEx (WE#) Hold from WE# (CEx) High
W7	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CEx) High
W8	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CEx) High
W9	t_{WPH}	Write Pulse Width High
W11	t_{VPWH}(t_{VPEH})	VPEN Setup to WE# (CEx) Going High

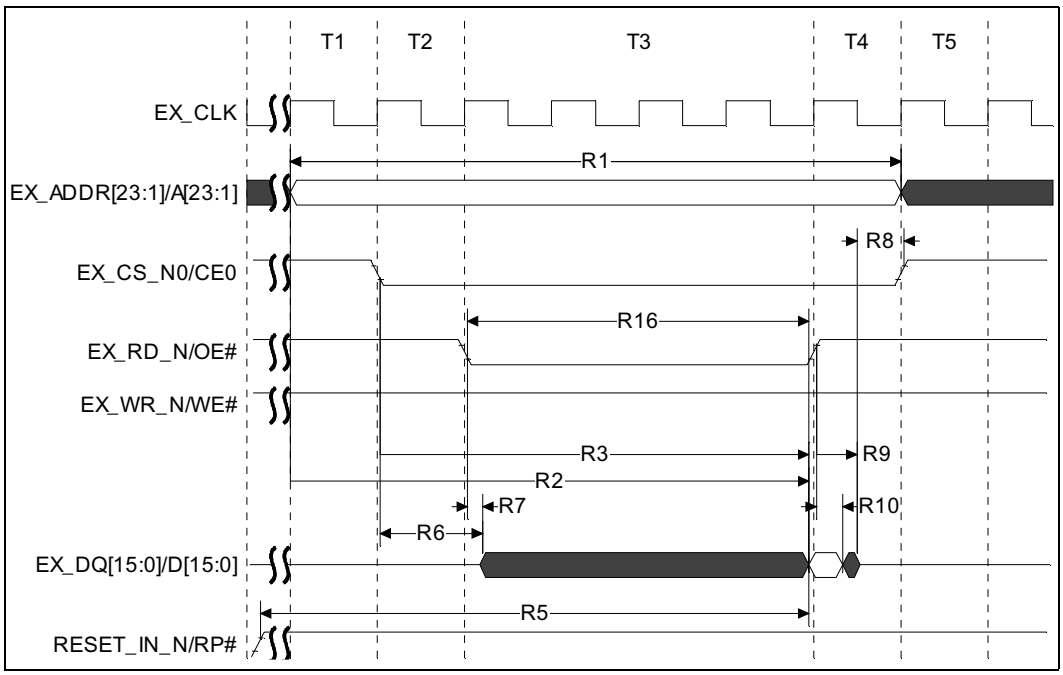
Note: For additional information regarding the individual components presented in this design example, consult the appropriate documents as listed in Appendix A, "Additional Information." Note that memory timings start with R (Read) or W (Write). Parameters in parentheses represent the field names of the SRAM Unit register settings, which determine the clock delays require.

6.1 Asynchronous Single - Word Read

Figure 3 shows the bus timings for an initial read following a reset.

Note: IXP42X Processor defaults to asynchronous read, so read accesses after a reset are always asynchronous reads. Non-array (register) reads are performed in this mode, as well.

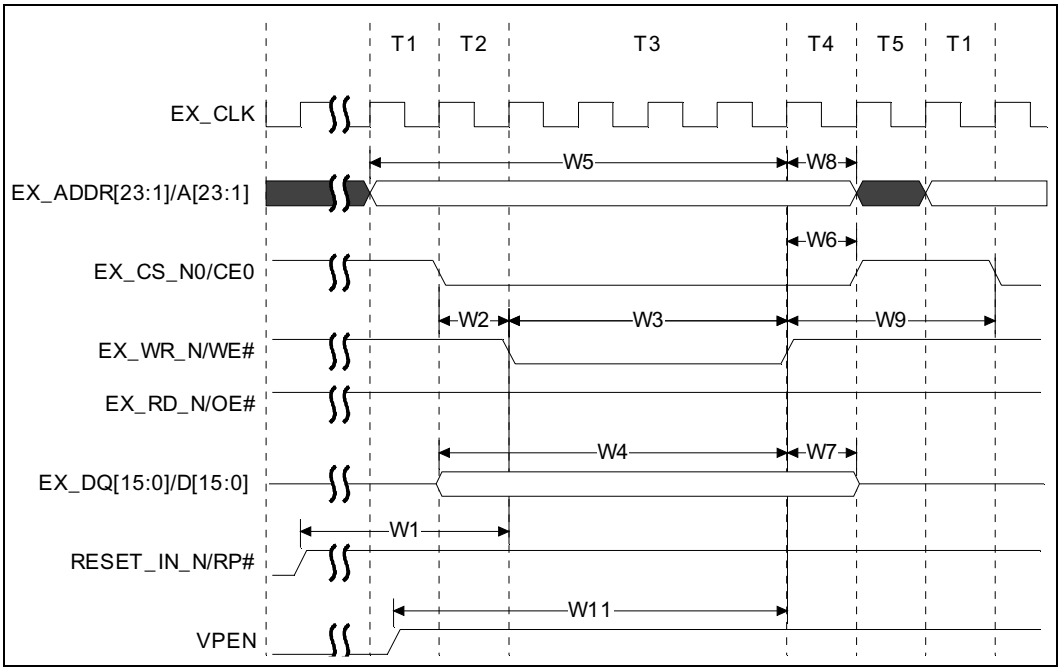
Figure 3. Asynchronous Single Word Read



6.2 Asynchronous Write

Figure 4 shows the bus timings for an asynchronous write to the J3 Flash Memory Device. Parameters in parentheses represent the register field names of the expansion bus register settings, which determine the clock delays required.

Figure 4. Asynchronous Write



7.0 Summary

The J3 Flash Memory Device provides 2X the bits in 1X the space by using reliable two-bit-per-cell storage technology. It is available in a variety of packages and densities for increased flexibility, and is an excellent option for both code and data applications where high density and low cost is required.

The flexible interface of the J3 Flash Memory Device gives the designer a simple "glueless" interface with processors such as the IXP42X Processor and the IXC1100 Processor, which helps to reduce power consumption, decrease systems costs, and increase overall system reliability by eliminating the need for additional interface components.

Appendix A Additional Information

Document Number	Document/Tool
290667	3 Volt Intel StrataFlash® Memory; 28F128J3, 28F640J3, 38F320J3 (x8/x16) Datasheet
252479	Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet
252480	Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual
252817	Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Network Processor Hardware Design Guidelines
297859	AP-677 Intel StrataFlash® Memory Technology
298130	3 Volt intel StrataFlash® Memory Specification Update
292222	AP-664 Designing Intel StrataFlash® Memory into Intel® Architecture
2512201	AP-757 Schematic Review Checklist for 3 Volt Intel StrataFlash® Memory
292221	AP-663 Using the Intel StrataFlash® Memory Write Buffer
292218	AP-660 Migration Guide to 3 Volt Intel StrataFlash® Memory
250260	AP-751 System Design Considerations When Designing with Intel® Flash
292172	AP-617 Additional Flash Data Protection Using VPP, RP#, and WP#
252702	Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Specification Update
300374	AP-792 Intel StrataFlash® Memory J3A to J3C Migration Guide (http://www.intel.com/design/flcomp/applnots/300374.htm)

NOTES:

1. Call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit the Intel World Wide Web home page http://www.Intel.com for technical documentation and tools.
3. For the most current information on Intel flash products, visit **http://developer.intel.com/design/flash/**.
4. See also the IXP42X documents at http://developer.intel.com/design/network/products/npfamily/docs/ixp4xx.htm.