Optimize FM transmission using digital PLLs

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More and more mobile devices such as MP3 players, PDAs, cellphones, personal media players and portable game consoles are carrying audio content. People have explored different wayswith or without wire-to transmit these audio signals to different external equipment, either to listen with a headset or share the content with others. Compared with other technologies, FM transmission provides an attractive alternative with a good balance of convenience, audio quality, power consumption and cost, as it has a huge receiver installation base and the technology is simple and proven.

The conventional FM transmitter consists of two basic modules (Figure 1). One is the stereo modulator that generates MPX signals; the other is the FM block that transmits FM signals. As required by the FM standard, the audio band signal has to be converted into an MPX signal and then modulated with an HF (76-108MHz) carrier. Usually, an analog PLL is used to generate and lock the HF carrier to a precise reference clock. The generation of the MPX stereo signal requires the proper addition and subtraction of the audio L/R signal and the composition of the 19kHz pilot tone. Certain pre-emphasis is also needed to generate the final MPX signal.

The MPX signal is directly coupled to the control voltage of the voltage control oscillator (VCO), thus modulating the phase/frequency of the carrier. Through a power amplifier, the FM signal is transmitted into the air.

There are three drawbacks to this pure analog approach. First, the direct modulation of control voltage requires a very narrow bandwidth PLL, which



Figure 1: Conventional FM transmitters have two basic modules: the stereo modulator and the FM block.

makes it very difficult to integrate the loop filter and VCO on chip due to the large passive devices needed and the poor on-chip VCO phase noise. This is the major reason why many external components are found in the traditional FM transmitter solution. As a fair amount of external passive components-including inductors, capacitors and resistors-require tuning and calibration before usage, it is a challenge for system vendors to control the quality and reliability of the system while keeping the cost low. Second, the precision of addition and subtraction in the analog amplifier is limited due to a mismatch of on-chip devices in the different signal paths. This will have a direct impact on the stereo

separation performance of the FM signal. Third, analog circuitry performance is limited by the device noise. SNR improvement comes with the penalty of power and area.

Overcoming drawbacks

A digital PLL and DSP-based FM transmitter architecture such as that implemented in the KT0801 can overcome such drawbacks.

Figure 2 shows the KT0801's architecture, which is based on a wide-band digital PLL that provides HF stability and high immunity to external noise and interference. Unlike existing products that directly frequency-modulate audio information in an analog domain, the KT0801 realizes frequency modulation, pre-emphasis, pilot tone and multiplexing in a pure digital domain.

The stereo audio signal is first amplified and filtered by the programmable gain amplifier (PGA) and low-pass filter (LPF) block. This connection can be either DC- or AC-coupled, since on-chip circuitry can provide DC biasing automatically if AC-couple is preferred. The 3dB frequency of LPF is set at about 20kHz no matter which gain is selected. LPF can filter out any HF noise from stereo sources and noise from the LPF itself. The PGA provides multiple gain settings so that the transmitter system can be customized for different audio sources. Very high linearity, low noise and low power consumption is realized by the KT0801 and its biasing



Figure 2: A digital PLL and DSP-based FM transmitter can overcome drawbacks of an analog approach.

calibration method.

After the amplification and filtering, the stereo audio message is digitized by $\Delta \Sigma$ ADCs, which is clocked by the on-chip crystal oscillator. $\Delta \Sigma$ ADCs are suitable for integrated audio applications because they can achieve very high analog performance at the cost of digital circuitry complexity. Besides the 20bit dynamic range performance, the most important issue about selecting the right architecture for the ADC is to make the charge drawn from the reference buffers to be signalindependent, as this will degrade the channel isolation directly. A low-power and low-noise reference buffer is also used for the conversion. The commonly used off-chip bypass capacitors are not necessary here. The dual channel analog front-ends are carefully designed to minimize gain and phase mismatch. An offset calibration is built to maximize dynamic range.

Digital filtering

The digitized results of $\Delta\Sigma$ ADCs are further filtered and decimated to minimize band noise, including quantization noise and input audio noise. Care is taken to make



Figure 3: A typical application circuit using KT0801 needs an external clock, a stereo signal source, a single signal source and an antenna.

sure that the passband ripple is minimized. A digital high-pass filter is also integrated on chip to filter out noise between DC and 20kHz. Since most of the signal processing is implemented in the digital domain, it is possible to have an accurate 3dB frequency for a digital high-pass filter without off-chip components.

Pre-emphasis is commonly adopted in digital audio systems because it can improve SNR performance for the whole system. Again pre-emphasis is executed in a digital domain to abstain the necessity of external components. The pre-emphasis time constant can be adjusted easily by setting a register. After the multiplexing signal is assembled in the digital domain, it is sent to the digital PLL for up-conversion.

Typical PLL needs external components for audio applications, since the interested audio band is fairly narrow. Also, it is very difficult to build a PLL with high linearity and wide tuning range suitable for all FM bands across process and temperature variations, as the on-chip devices have limited linearity and other non-ideality. KT Micro has also built a set of proprietary circuits and calibration schemes to cope with such issues. The measurement result shows that the design achieves better than 68dB SNR on a tuning range of 76-108MHz.

As illustrated in **Figure 3**, the KT0801 just needs an external clock, a stereo signal source, a single signal source and an antenna to make a high-quality low-cost portable FM transmission solution.