A closer look at SED, FED technologies

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The information display is a critical human interface to electronic systems. Industry experts have been working for decades to make them larger, lighter, brighter and thinner particularly for TV use. Furthering the quest for the exemplary display TV is the introduction of HDTV. HDTV provides means for transforming the entertainment experience. By delivering crystal clear video in high resolution, high-fidelity surround sound, full-screen graphics and the ability to drive interactive applications, HDTV delivers an immersive user experience that is attracting consumers all over the world.

Due to the inherent flaws in current display technology for HDTV, many researchers have turned to field emission display (FED), which uses carbon nanotubes (CNTs) to emit electrons, as the technology of choice for HDTV. It is this technology that will be able to support the HDTV revolution at an acceptable cost. On the other hand, Canon and Toshiba have developed another class of FED that is based on a lateral field emitter called the surface-conduction electron-emitter display (SED). We have classified the SED in the FED family for two reasons. First, the Society for Information Display and other display conference organizers generally place SED presentations and posters together with FED talks; we will be consistent with this convention. Second, there are many things that the FED and SED have in common. This article discusses the similarities and differences between the two technologies, and their effect on performance.

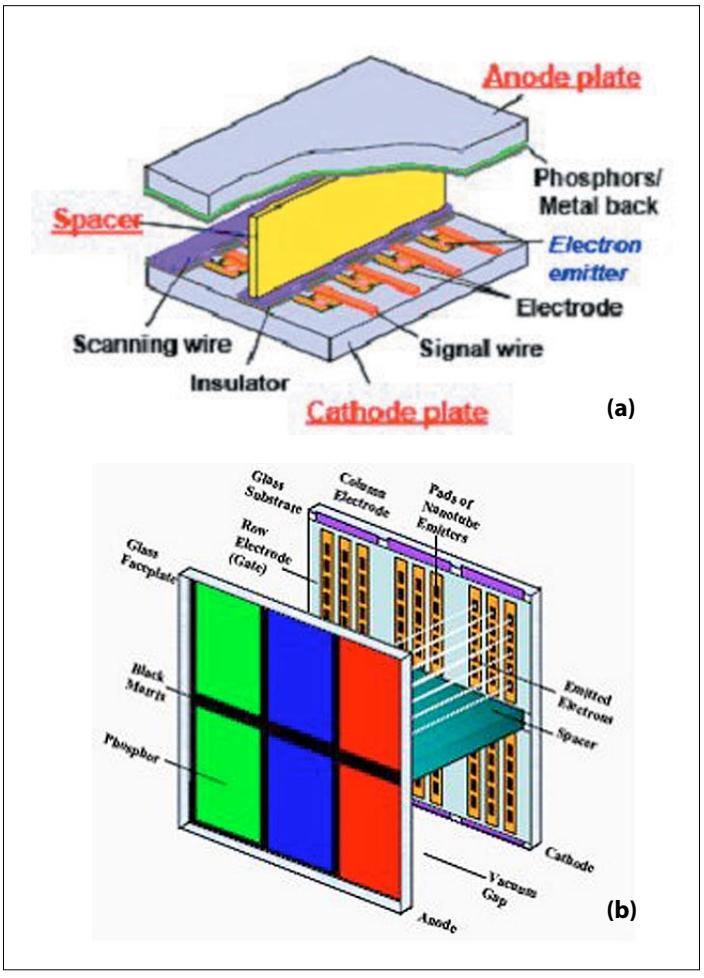

Figure 1: The structure for FED (b) is similar with the structure of SED (a) except for the details of the cathode plate.

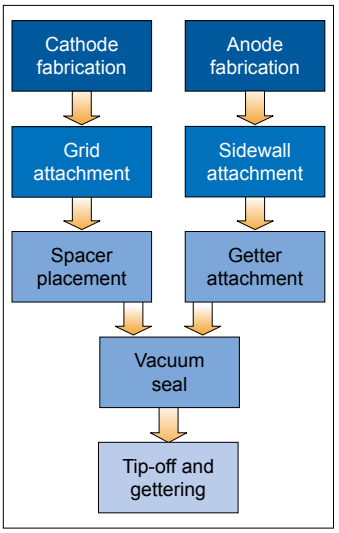

Figure 2: Shown is the basic flow of display fabrication.

Common characteristics

SED and FED technologies have many things in common in terms of form factor, view technology, structure and manufacturing.

Form factor—They are both flat- and thin-screen technologies that—depending on the approach—can achieve HDTV specifications for large-screen displays. In the International Display Workshops Proceedings 2005, a 36-inch diagonal SED panel was described as having 1,280 x 3 x 768pixels. This display is only 7.3mm thick, which sums up the 2.8mm cathode plate, 2.8mm anode plate and 1.7mm vacuum spacing. The panel weight is 7.8kg. The weight and thickness of an FED of comparable size is expected to be about the same. The target market for both FED and SED is large-area HDTV.

View technology—SED and FED are both direct-view or emissive display technologies. Each pixel or sub-pixel generates its own light energy that is seen directly by the viewer, allowing high contrast and efficiency, and other performance improvements. For SED and other FED technologies, the light that forms the image is created by energetic electrons striking a phosphor screen anode, very similar to the anode screen of a CRT. The phosphors used are also

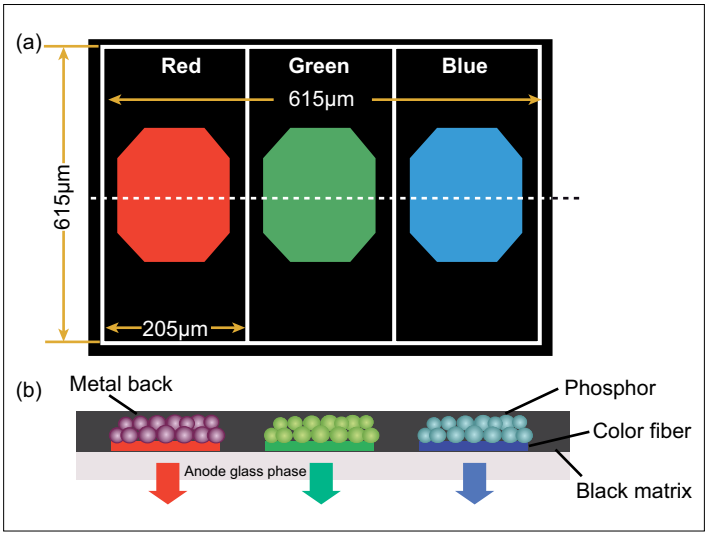

Figure 3: The anode fabrication process is very similar for both SED and FED.

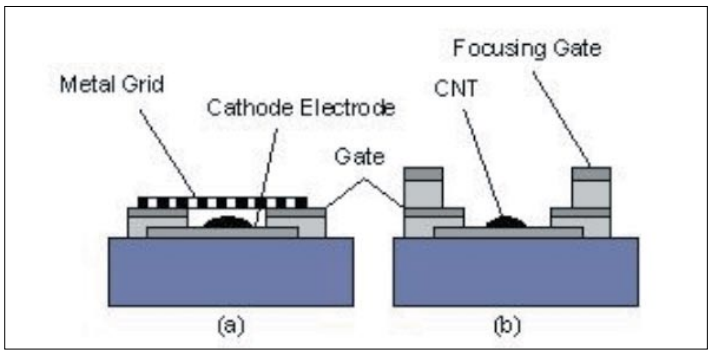

Figure 4: A metal grid is suspended over the CNT electron-emitter patch that sits on top of a cathode line (a). The gate structure is fully integrated and photolithographically formed on the cathode plate (b). This design also exhibits additional focusing electrodes to help control the electron beam width.

the same or very similar to those used in CRTs.

Structure—Electron acceleration requires a vacuum to avoid corona or plasma discharge. Thus, the mechanical structure of the SED and other FEDs consists of a hermetically sealed glass envelope that is evacuated to form the vacuum space required to accelerate the electron beams. Depending on the size of the display and thickness of the glass walls, spacers are generally required in order to support the glass walls against the atmospheric pressure. The spacers must also be able to stand off high voltage gradients and be optically invisible to viewers under normal operating conditions. The 36-inch SED required 20 rib-type spacers to maintain the 1.7mm vacuum gap. A schematic of the SED display is shown in **Figure 1**. FED displays have been demonstrated with both rib-type and post-type spacers. Furthermore, all FED technologies—including SED—require a form of getter technology to maintain the required vacuum inside the glass envelope after the display is evacuated and sealed.

Manufacturing—Their fabrication and assembly approaches are also very similar except for the cathode plate, which will be described later. All FED approaches being developed today require assembling a face-plate (anode) with a back-plate (cathode or electron source), together with sidewalls, spacers and getters. First, the anode and cathode plates are fabricated separately, assembled with the other components, sealed using glass frit or other novel materials and then evacuated. **Figure 2** diagrams the assembly process for a CNT-based FED, but can be applied to other FED technologies, including SED. In some approaches, the sealing and evacuation steps are combined, and still other approaches hope to eliminate or reduce the number of spacers. New materials are under development to replace frit-glass seals in order to lower the sealing temperature and to avoid materials with high lead content.

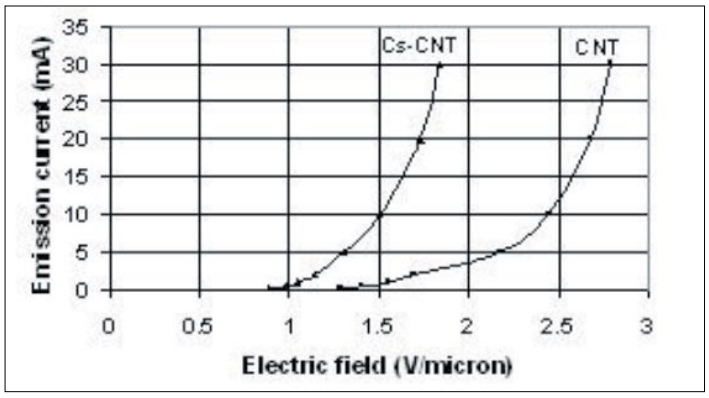

Figure 5: The current from the emitter as a function of the applied voltage is highly nonlinear. Cesium lowers the workfunction and allows emission at lower extraction fields.

The anode fabrication process is very similar for both SED and FED. **Figure 3** shows the details of the anode configuration for an SED panel. The black matrix and color filters are used to improve contrast. The metal back film is used to improve brightness and efficiency, and also acts as an electrode for the high voltage potential and bleeds charge away from the phosphor during e-beam illumination. These are standard technical modifications used in CRT, FED and high-voltage vacuum fluorescent display to improve the performance of the phosphor.

Finally, both SED and CNT-based FED displays have used printing to fabricate the anode and cathode plate, as will be detailed in the following section. Thus depending on your point of view, the SED and other FED technologies have many components in common, such as the anode and phosphors used on the anode, spacer technology, getters and much of the assembly process. Now let's look at what is unique to SED and other FED technologies.

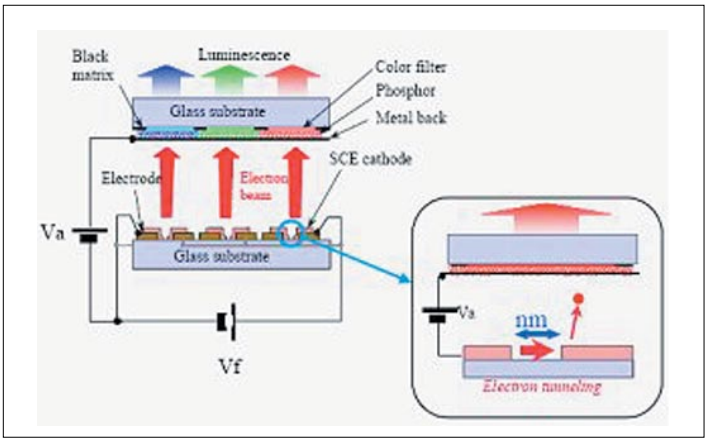

Figure 6: Each sub-pixel has a unique pair of electrodes that supplies an electron current.

Technology distinctions

The significant differences between SED and FED are clearly seen in the electron source plate and the drive electronics. Before we discuss the significance of the differences, we must first understand how each is structured and operated.

Standard FED emitter configurations—Some typical configurations using CNT emitters are shown in **Figure 4**. Microtip emitters have similar configurations as CNT. In either case, electron beams are created by extracting electrons from the emitter structure (CNT or microtip) as a result of the high electric fields applied to the emitter from voltage differences between the anode, gate and cathode electrodes. In some cases, the anode field contributes to the electron emission, but the cathode-gate voltage difference controls the emission current intensity.

Electron current from the FED emitters is controlled by the field applied to the emitter as a result of the cathode to gate bias and is governed by the Fowler-Nordheim equation. The current from the emitter as a function of the applied voltage is highly nonlinear. An example of the I-V characteristics for a CNT emitter is shown in **Figure 5**. In addition to the applied field, the emission current is also dependent on the workfunction () of the emitter and the shape of the emitter. As the workfunction is decreased such as with a coating of alkali metal, it is easier to extract electrons at lower fields. As the shape of the emitter becomes sharper, it is also easier to extract electrons since the local electric field is higher at the point of the emitter.

There are two important points to make concerning the standard FED approaches. Firstly, the configuration is largely vertical. Typically, the gate is placed

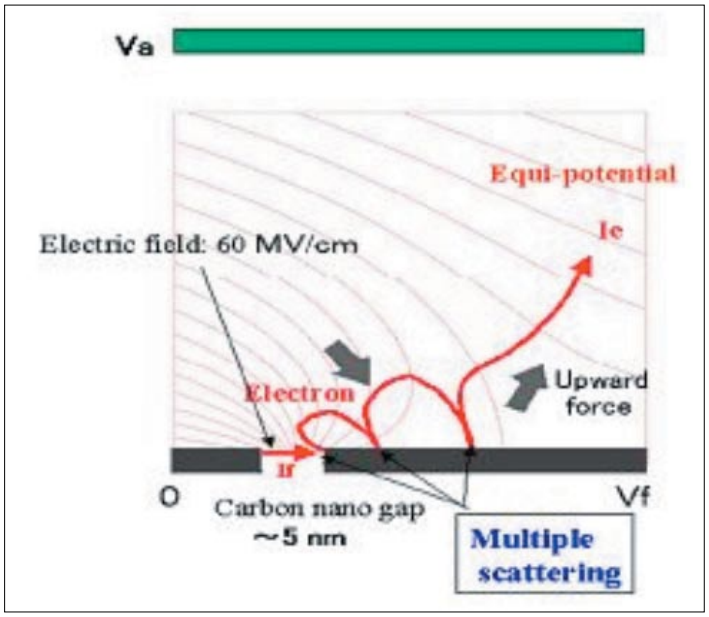

Figure 7: The electrons that tunnel across the gap and strike the counter-electrode are either absorbed into the counter-electrode or scattered, captured by the electric field created by the anode potential and accelerated to a particular phosphor dot.

near the cathode electrode, such that the applied electric field is mostly vertical at the cathode electrode where the CNT emitter is deposited. The electrons that are emitted from the cathode travel directly to the anode. Some broadening of the beam takes place as a result of the lateral components of the applied field, but these are limited as much as possible by the design or are corrected with additional focus electrodes placed in the path as needed. The typical goal of the FED designer is to prohibit the electrons from striking any other surface other than the anode after the electrons leave the emitters. The SED emitter includes a multiple-scattering process.

Secondly, typical FEDs are voltage-drive devices. In a passive matrix FED display, it is difficult to apply more than two or three voltage levels between the cathode and the gate (ON and OFF voltages), so gray scale in the image is achieved by pulse width modulation (PWM). As for all passive matrix flat-panel displays, the image is created line-by-line. As one line is activated, the pixels in that line are switched ON by the column drivers; the period that each pixel in the line is left ON is determined by the luminous intensity required from that pixel for that image frame. Since the emission current from the emitters is highly nonlinear and the fabrication of the emitters is difficult to control, emission uniformity and thus image uniformity are the major problems to overcome for microtip and CNT displays. Fabrication techniques have improved the uniformity of CNT-based FEDs. Often, emission uniformity across the cathode is controlled by a current feedback resistor placed in line with the cathode electrode.

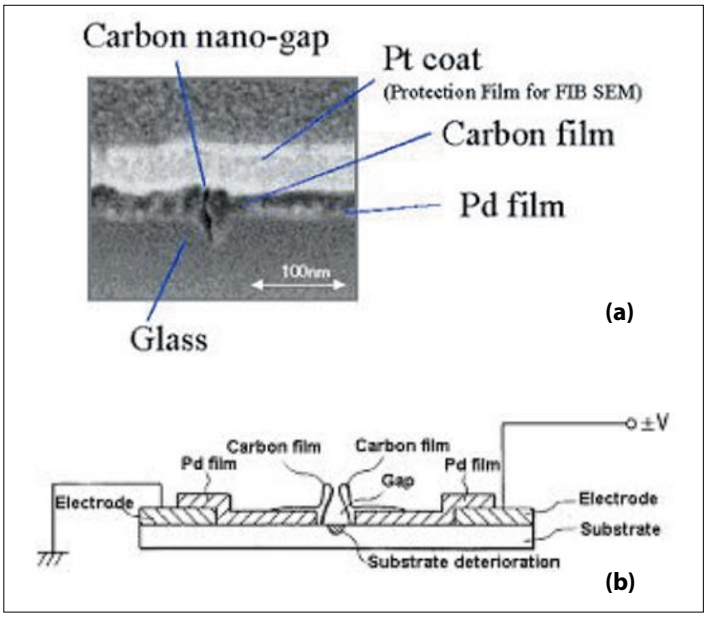

Figure 8: Shown is the SEM cross section image of the carbon nano gap fabricated by the forming and activation processes (a).The substrate deterioration is a result of the high temperature created locally by the activation process (b).

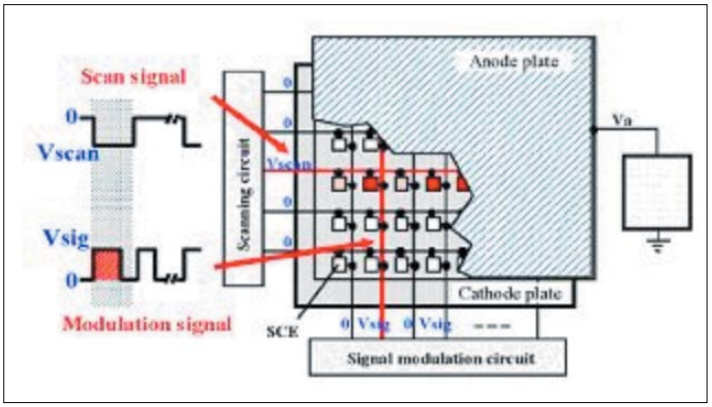

Figure 9: The SED is driven line-by-line.

Fabrication of FED emitter is a dependant of the approach taken by the FED development team. Motorola and LETI have developed processes that require CNT growth directly on the cathode substrate, while groups like ANI and Samsung have developed processes that allow printing of the CNT. Printing approaches are more favorable for fabricating large area cathodes with uniform emission in high volume as opposed to high-temperature chemical vapor deposition (CVD) approaches required for direct CNT growth. The printing approaches require an activation step, but even this has been optimized for large-area fabrication using a bead-blasting technique.

SED structure—This is unique to other FED approaches, in that the electron beam current supplied to the anode for each pixel is generated in a two-step process.

In the first step, the electron source operates by first emitting electrons laterally (parallel to the cathode substrate) across a very narrow gap formed between two electrodes. The gap between the electrodes, although small (on the order of a few nanometers), is still a vacuum gap that requires application of an electric potential to extract electrons from one electrode through the vacuum tunneling barrier to the other electrode. The current across the electrode gap follows the Fowler-Nordheim law and is thus highly nonlinear, allowing for matrix addressability. This lateral emitter structure is where the term surface conduction emitter (SCE) comes from. **Figure 6** is a diagram of the SED emitter structure.

In the second step, the electrons that tunnel across the gap and strike the counter-electrode are either absorbed into the counter-electrode (thereby creating only heat and no light) or scattered, captured by the electric field created by the anode potential and accelerated to a particular phosphor dot. Thus, it creates a spot of red, green or blue light. This combined electron emission plus electron beam scattering process is illustrated in **Figure 7**, where Va is the anode potential and Vf is the driving potential across the gap. Multiple scattering events may take place before the electron is captured by the anode field. The efficiency of the number of electrons captured by the anode field (Ie/If, Figure 7) is quite low, on the order of 3 percent, but the power efficiency

is reasonable since Vf is low, on order of 20V. Note also that the uniformity of electron current reaching that anode depends on field emission current at the gap convoluted with the efficiency of scattering events from pixel-to-pixel.

The emitter described in Figure 7 is fabricated using a combination of technologies. The simple matrix wires are deposited by a printing method using silver wires and insulating films at the crossovers. Platinum (Pt) electrodes are formed using thin-film lithography. The gap between these electrodes is 60m. The carbon nano gap is created in a two-step process, beginning by depositing a palladium oxide (PdO) film (10nm thick) by ink-jet printing over and between the Pt electrodes. This film is composed of ultrafine particles of PdO of diameter about 10nm. First, a gap is "formed" in this film by reducing the oxide by passing a series of voltage pulses across this PdO film between the two Pt electrodes. The PdO is reduced by the heat of the pulses as the substrate is in a vacuum environment. As the PdO is reduced, the film is stressed and eventually a sub-micron gap is formed across the diameter of the PdO dot. Second, the gap is "activated" by exposing the cathode to an organic gas, and more pulse voltages are applied across the gap. These pulse voltages create a local discharge that leads to CVD-like deposition of a carbon film in the gap, such that the gap narrows to a self-limiting distance of order 5nm. When the gap is large, carbon material is deposited as a result of the disassociation of the hydrocarbon molecules in the plasma resulting from the discharge. As the gap becomes smaller, the local discharge current created by the pulse becomes large and material is evaporated. At a gap of about 5nm, deposition and evaporation of carbon material reaches equilibrium. The width of this gap is controlled by the pressure of the organic gas and the pulse voltage. A cross section image of this gap is shown in **Figure 8**.

Similar to the FED, the SED is driven line-by-line (**Figure 9**). The scanning circuit generates the scan signal (Vscan), and the signal modulation circuit generates a PWM signal (Vsig) that is synchronized with Vscan. Because of the highly nonlinear Ie-If characteristics of the surface conduction emitter, it is possible to drive each pixel selectively using a simple matrix x-y configuration without active elements and still achieve a luminance contrast ratio of 100,000:1 with a signal voltage of 18.9V and a scanning voltage of 9.5V. Contrast these values with a typical signal voltage of 35-50V and scanning voltage of 50-100V for CNT-based FED structures. The SED switching devices are much lower voltage, but they must be designed for much higher steady-state current loads, as much as a factor of 30 or higher as a result of the inefficiency of the SCE electron scattering mechanism. The larger currents of the SED also forces the interconnect lines to have lower resistances compared with FED, as even a small voltage drop along the line can result in edge-to-edge non-uniformity.

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