

AN-8013

FMS6418B Evaluation Board Application Note

Description

The FMS6418B evaluation board provides a flexible base for evaluating the performance of the FMS6418B. The FMS6418B evaluation board operates from a standard supply voltage of +5V ±5%.

The FMS6418B offers comprehensive filtering for set top box or DVD applications. This part consists of a triple 6th order filter with selectable 33MHz or 8MHz frequencies.

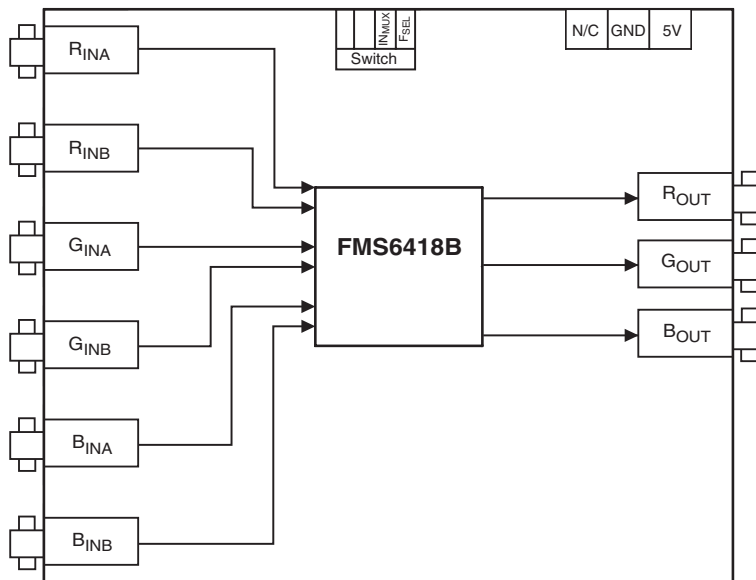
2-to-1 multiplexers are provided on the triple filters. The triple filters are intended for either YUV or RGB signals. All channels accept DC coupled ground-referenced 1V_{pp} signals. The filters output 2V_{pp} signals into AC coupled terminated loads. The low-pass filters are powered by 3.3V and the outputs by 5.0V.

Applications

- Cable set top boxes
- Satellite set top boxes
- DVD players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

For a complete description of the FMS6418B please refer to the FMS6418B data sheet.

Evaluation Board Block Diagram



Evaluation Kit Contents

The FMS6418B Evaluation Kit contains the following items:

- AN-8013 – FMS6418B Evaluation Board Application Note
- The latest revision of the FMS6418B data sheet, which also can be obtained from <http://www.fairchildsemi.com>.
- Fully functional FMS6418B eval board
- Female power connector

Board Setup and Test

The following test equipment is necessary to test the FMS6418B eval board.

- One power supply +5V ±5%, 250mA
- One high resolution CRT monitor (2 channel with RGB)
- One HDTV
- One NTSC or PAL video signal source capable of generating necessary outputs
- One video measurement set (VM700)
- VM5000HD video measurement set
- Assorted video cables

Use the following procedure to verify that the FMS6418B eval board is functional. This only verifies functionality. These instructions do not test any parameters outlined in the data sheet.

SD Verification

1. Verify that the switches are in the correct position.
2. SW1-1 and SW1-2 should be off. SW1-3 and SW1-4 are not used. All toggles should be in the up position.
3. See Table 1 for switch configurations.

Table 1. Switch Setting for RGB Channels

Control		Outputs		
IN _{MUX} (SW1-2)	F _{SEL} (SW1-1)	R _{OUT}	G _{OUT}	B _{OUT}
Off (up)	On (down)	R _{INA} (SD)	G _{INA} (SD)	B _{INA} (SD)
On (down)	On (down)	R _{INB} (SD)	G _{INB} (SD)	B _{INB} (SD)
Off (up)	Off (up)	R _{INA} (HD)	G _{INA} (HD)	B _{INA} (HD)
On (down)	Off (up)	R _{INB} (HD)	G _{INB} (HD)	B _{INB} (HD)

DO NOT turn on power supply until all connections are completed.

1. Set the power supply to 5.0V. Connect the power supply to the input voltage terminals of the evaluation board.
2. Connect RGB signal source to the appropriate input BNC connectors. (RGB_{INA})
3. Connect the appropriate monitor cables to the output BNC connectors. (RGB_{OUT})
4. Turn power on.
5. Press RGB channel on monitor and verify test pattern as the same going into RGB_{IN}.
6. Switch SW1 on (down) and verify loss of signal.
7. Switch BNC cable to RGB_{INB} and verify the signal is back.
8. Testing is now complete.

HD Verification

1. Configure the switches as outlined in Table 1 for HD Mode
2. Connect HD signal source to the appropriate input BNC connectors. (RGB_{INA})
3. Connect the appropriate HDTV cables to the output BNC connectors. (RGB_{OUT})
4. Turn power on.
5. Verify test pattern is displayed on the monitor.
6. Switch SW1-1 down and verify loss of signal.
7. Switch BNC cables to RGB IN B and verify the signal is back.
8. Testing is now complete

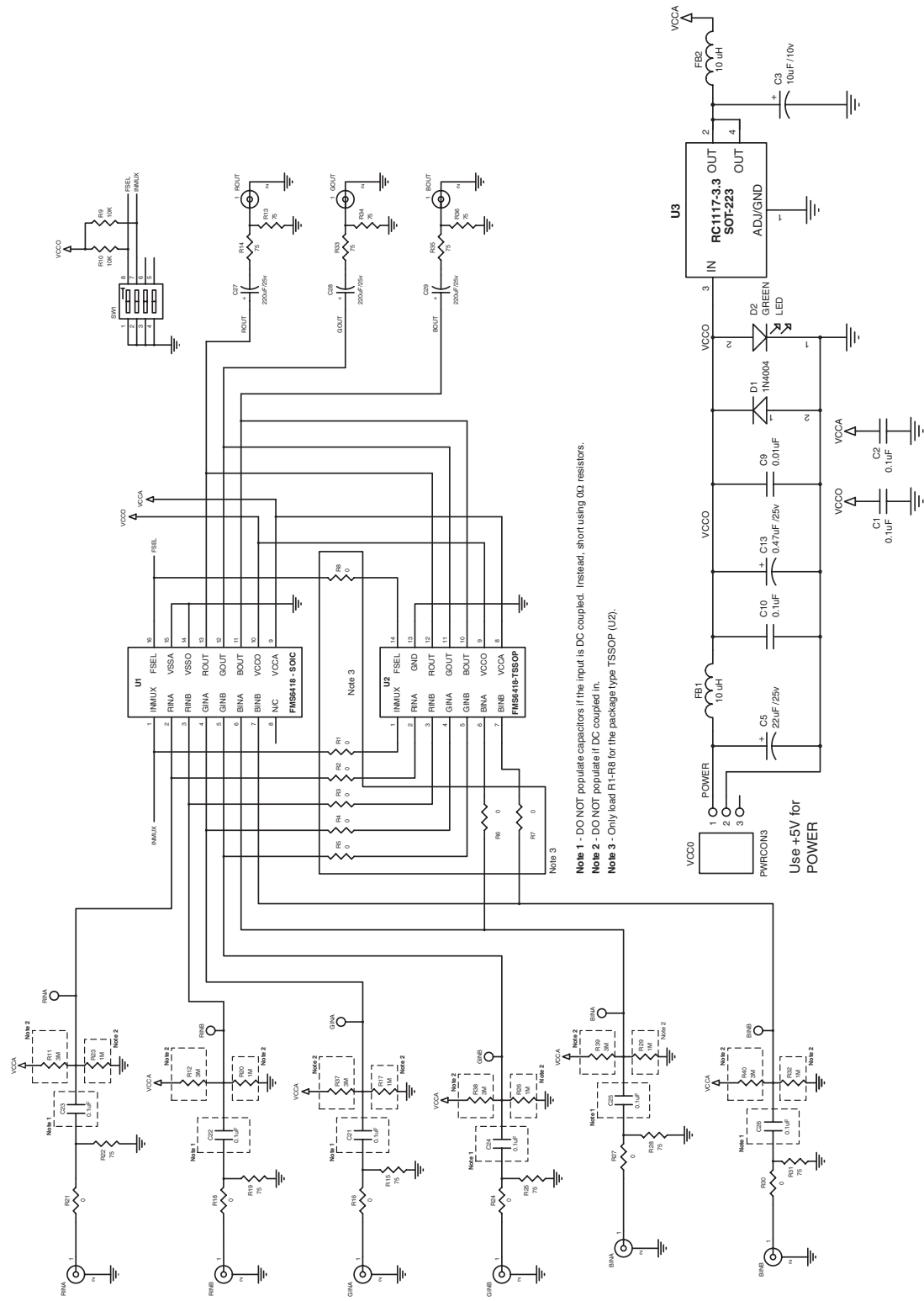


Figure 1. FMS6418B Schematic Diagram

Bill of Materials

Item	Quantity	Reference	Part
1	6	R _{INB} , R _{INA} , G _{INB} , G _{INA} , B _{INB} , B _{INA}	TP
2	9	C1, C2, C10, C21, C22, C23, C24, C25, C26	0.1 μ F
3	1	C3	10 μ F/10V
4	1	C5	22 μ F/25V
5	1	C9	0.01 μ F
6	1	C13	0.47 μ F/25V
7	3	C27, C28, C29	220 μ F/25V
8	1	D1	1N4004
9	1	D2	Green
10	2	FB1, FB2	10 μ H
11	1	J1	RINA
12	1	J2	RINB
13	1	J3	BINB
14	1	J3	BINA
15	1	J3	GINA
16	1	J3	GINB
17	1	J4	ROUT
18	1	J5	GOUT
19	1	J6	BOUT
20	14	R1 thru R8, R16, R18, R21, R24, R27, R30	0
21	2	R9, R10	10k
22	6	R11, R12, R37 thru R40	3M
23	12	R13, R14, R15, R19, R22, R25, R28, R31, R33 thru R36	75
24	6	R17, R20, R23, R26, R29, R32	1M
25	1	SW1	SW DIP-4
26	1	U1	FMS6418B-SOIC
27	1	U1	FMS6418B-TSSOP
28	1	U3	RC1117-3.3
29	1	VCCO	PWRCON3

Applications

DC Levels

At any given time, the input signal's DC levels must be between 0.0V and 1.3V to utilize the optimal headroom and to avoid clipping on the outputs.

DC Coupled Output Applications

The 220 μ F capacitor coupled with the 150 Ω termination forms a high pass filter that blocks the DC while passing the video frequencies and avoiding tilt. Lower values such as 10 μ F would create a problem. By AC coupling, the average DC level is zero. Thus, the output voltages of all channels will be centered around zero. Alternately, DC coupling the output of the FMS6418B is allowable. There are several trade-offs: The average DC level on the outputs will be 2V; each output will dissipate an additional 40mW nominally; The application will need to accommodate a 1V DC offset sync tip; And it is recommended to limit one 150 Ω load per output.

Driving the Digital Pins with 3.3V or 5V Logic

Either is allowed as long as the V_{IH} and V_{IL} are adhered to.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. Fairchild offers the FMS6418BDEMO evaluation board to use as a guide for layout and to aid in device testing and characterization. The FMS6418BDEMO is a 4-layer board with a full power and ground plane. Following this layout configuration will provide the optimum performance and thermal characteristics. For optimum results, follow the steps below as a basis for high frequency layout.

- Include 10 μ F and 0.1 μ F ceramic bypass capacitors.
- Place the 10 μ F capacitor within 0.75 inches of the power pin
- Place the 0.1 μ F capacitor within 0.1 inches of the power pin
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For 2 layer boards, use a ground plane that extends beyond the device by at least 0.5 inches
- Minimize all trace lengths to reduce series inductance

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