A Low-Power High-precision Self-testing Data Acquisition System for a Large Seismic Exploration Grid

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Abstract

In seismic exploration for oil and gas, a grid of 2,000 to 30,000 nodes is formed to acquire reflected wave signals from the rock layers in the earth. Each node consists of a sensor, complete data acquisition system with self-test, and telemetry for returning data to a central recording unit. This demanding application requires a highly linear, wide dynamic range data acquisition system with a 0.1 - 200 Hz bandwidth. A large number of nodes operating simultaneously require that each node consume very low power. The components of each data acquisition node are: a geophone or a hydrophone (sensors for land and marine exploration respectively), a programmable gain differential amplifier, a delta-sigma analog to digital converter, a multi-function decimation filter, and a high precision DAC for calibration and self-test. Each of these components is optimally designed for low power in large sensor arrays. The acquisition node requires self-calibration capability and operation in a synchronous mode where all channels acquire data simultaneously. A data acquisition system that meets these requirements has been designed and tested. The overall performance of the system is better than 112 dB linearity (THD) and 123 dB dynamic range (SNR) at 500 SPS. The power consumption for the data acquisition portion of a single node is 105 mW from a 5V analog power supply.

1 Introduction

Seismic exploration for gas and petroleum involves generation of seismic waves using either a dynamite blast or a vibrating thumper truck in the case of land exploration, or air guns in the case of marine exploration; and acquiring the reflected waves from the rock layers in the earth to create a map of the underground structures. Very early seismic data acquisition systems in the 1980's used an instantaneous 'floating point' amplifier with automatic gain control (AGC) along with 12 to 16 bit successive approximation analog to digital converters. However, the dynamic range of these early systems was limited to about 70db.[1] Moreover, the maximum number of channels in the system was fewer than 480 due to limitations in real-time data collection. In the late 1980s, channel counts increased to a maximum 8000 channels, supporting the industry progression from 2D underground maps to 3D maps. [3]

With the introduction of delta sigma converters in the early 90s, data acquisition resolution increased dramatically from 16 bits to 24 bits, yielding 120dB of dynamic range. The increased dynamic range greatly improved the image quality by resolving previously unseen underground structures.

The surface area over which the sensors are deployed, called the grid, has steadily increased in size and channel count over time. Land grids now exceed a few square kilometers, and marine grids exceed 10 kilometers in length At the present time, for example, a typical marine grid consisting of 8 marine streamers is 7680 acquisition channels and is 12

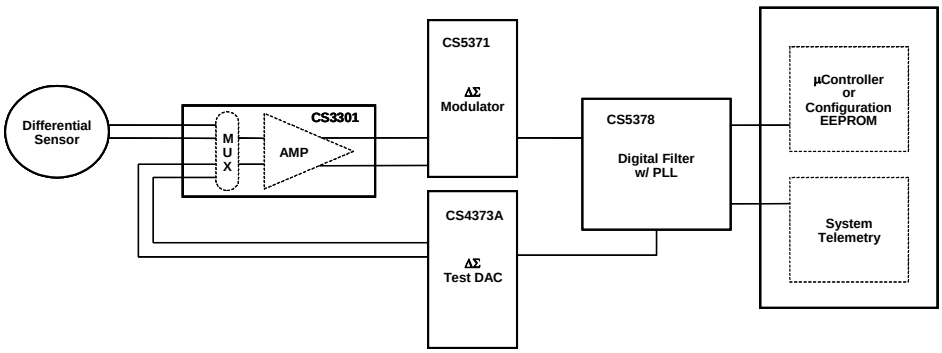

Figure 1 Seismic Single node data acquisition system

kilometres long.[3] The channel count and channel density for marine as well as land exploration is also on the rise. The future trend is to increase the channel counts to over 30,000 per system.

As much land exploration is done in very inhospitable environments, a very low power data acquisition channel is desirable to reduce the number of deployed batteries. These channels are required to have a wide dynamic range, high linearity, and be capable of self-test before each acquisition to ensure the integrity of the data collection system. In addition to these individual requirements, each channel must be calibrated and synchronized to meet precise gain and phase accuracy limits relative to others in the system.

2. Seismic Data Acquisition System

The data acquisition channel is illustrated in Figure 1. A differential sensor (geophone or a hydrophone sensor for land and marine exploration respectively) is connected through a programmable gain instrumentation amplifier (PGIA) to the ΔΣ modulator, where analog to digital conversion occurs. The modulator's 1-bit output connects to the multi-purpose filter, where the oversampled ΔΣ data is decimated and filtered to 24-bit output samples at a programmed output rate. These output samples are buffered into an 8-deep data FIFO and then passed to the system telemetry. System self tests are performed by connecting the test bit stream (TBS) generator within the filter block to the test DAC. Analog tests drive differential signals from the test DAC into the multiplexed inputs of the PGIA or directly to the differential sensor. Digital loopback tests internally connect the TBS digital output directly to the 1-bit data input of the filter block to check the integrity of the filter functions

3. Programmable Gain Instrumentation Amplifier (PGIA)

The signal strength from the sensor varies with its distance with respect to the source. The full scale of the ADC is utilized by amplifying the received signal using the PGIA. Figure 2 illustrates the internals of this PGIA. The gain settings are binary weighted from 1X to 64X. Each amplifier in this PGIA is chopper- stabilized to remove offset voltage and remove the effects of 1/f noise. The input referred noise of this amplifier is 8.5 nV/sqrtHz from 0.1 to 2000Hz.

This PGIA achieves very high linearity (118dB) even when set for 36dB gain. This is possible because the amplifier uses a unique multi-path feed forward architecture. [6] Class AB output stage is used for the drive capability and power saving. However, the non-linearity penalty of class AB stage is minimized by the very high open loop gain of the amplifier. This particular multi-path feed forward architecture was selected to obtain 180dB open loop gain at 200Hz bandwidth with a small operating power (27.5 mW).

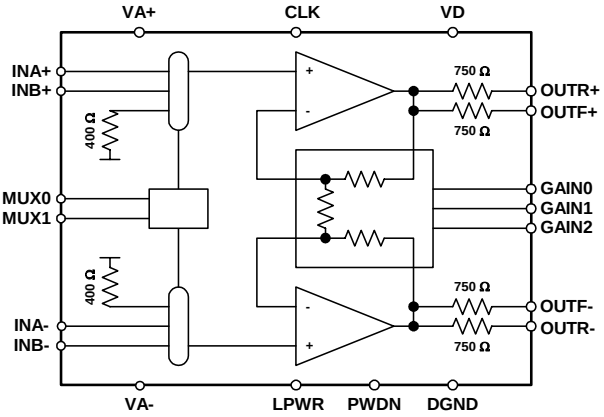

Figure 2: Block diagram representation of PGIA

The open loop gain and phase plots for this amplifier are shown in Figure 3. Curve A shows the gain and phase plots for a dominant pole amplifier, while curve B is for a multi-path feed forward compensated amplifier. This clearly shows the reduction in unity gain band width for the multi-path feed forward compensated amplifier, thus saving power.

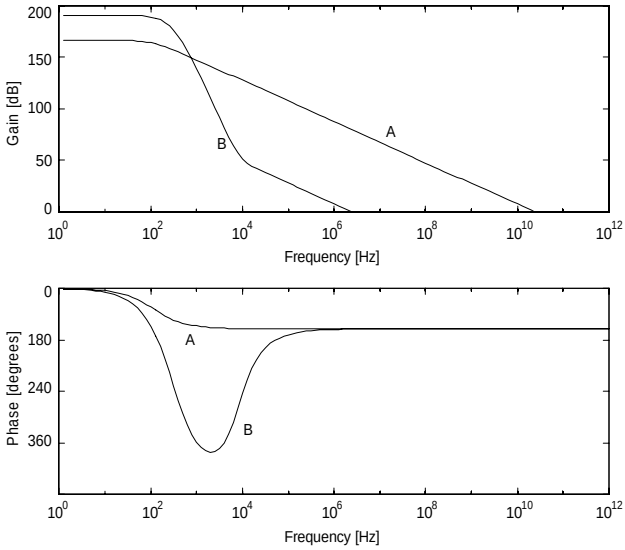

Figure 3: Gain and phase plots for (A) dominant pole amp, and (B) multi-path feed forward compensated amp.

The instrumentation amplifier is especially designed for seismic applications. The input MUX can select input A for the main signal flow; input B for channel calibration; and internal termination (800 Ohms) to determine the noise performance of the channel. A companion amplifier, which is designed with similar power and noise specifications but without chopper stabilization interfaces to a high impedance hydrophone. The 1/f corner for this amplifier is ~10Hz.

4. Delta Sigma Modulator (ADC)

A fourth order single bit delta sigma modulator as shown in Figure 4, is used in this design. The performance of the ADC is predominantly determined by the first integrator and the feedback DAC. Hence a big portion of the power budget of this modulator is utilized in the first integrator to maximize the linearity, and to minimize the noise. In this design, significant power savings were achieved by the proper choice of the modulator coefficients, and also by dynamically biasing the first integrator. A rough/fine charge sampling scheme is used to reduce distortion caused by nonlinear input currents. Fully differential circuits are used in all blocks, to reduce noise pickup and maximize linearity.

The choice of the modulator coefficients has a direct impact on the power consumption, as the coefficients determine the size of the circuit elements to be used in the design. By using large over-sampling ratios (OSR) it is possible to generate coefficients optimized for power, and still meet the required performance. The input-referred noise of the sampling capacitor structure as shown in Figure 5 is given as,

$$Vn^2 = \frac{4KT(1 + Cref/Cin)}{Cin.OSR} \qquad (1)$$

At higher OSR, (in this design OSR=512) the capacitance Cin and Cref can be reduced, which results in the increased bandwidth and slew requirements on the first integrator, but still meet the noise performance. Maximizing the 'Cin/Cref ' ratio has a two-fold advantage: First it reduces the noise as shown in equation (1). Second, it reduces the total capacitive loading on the amplifier, and maximizes the feedback factor, which would mean faster settling for a given operating power.

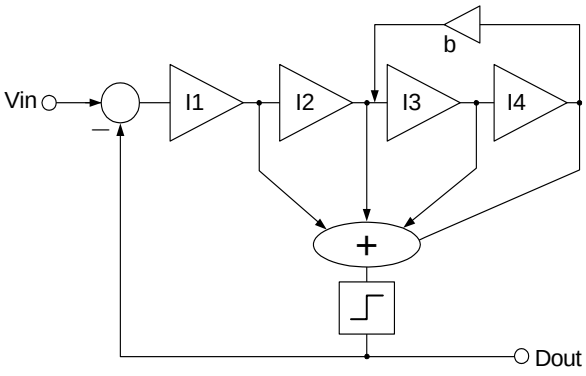

Figure 4 Single-bit fourth order ΔΣ modulator

Another substantial power saving can be achieved by maximizing the gain of the first integrator. It makes the amplifier design more challenging, but reduces the capacitive load 'Cpar', which is the backplate capacitance of the integrating capacitor 'Cint' on the amplifier. A lower capacitive loading will result in power savings as the amplifier transconductance can be proportionally lowered for a given bandwidth.

A clocked biased class-A amplifier was used in the first integrator to optimize the power dissipation for each phase, independent of the signals present. The amplifier of the first integrator has three distinct tasks to perform, viz. slewing, settling and holding an output value.

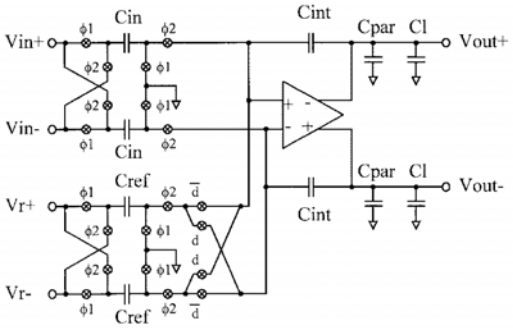

Figure 5 Sampling network for the ΔΣ modulator

In phase2 the amplifier has to slew and then settle to the final value. The error voltage Ve(t) after settling a disturbance is given by,

$$Ve(t) = Vi.\exp(-t.gm/Cleff) \qquad (2)$$

$$Cleff = Cpar + Cin\,(1 + Cref/Cin) \qquad (3)$$

where 'gm' denotes the transconductance of the input pair. To meet the power dissipation it was needed to increase the time available for settling. This can be achieved by increasing the current in the amplifier during the portion of the phase2, where slew could be expected. The work performed during slew is,

$$W = \frac{Io.\,V\,.\,tslew}{2} \qquad (4)$$

where Io is the output current, V the voltage the capacitance is discharged over, tslew the total slew time. Equation (4) shows that a higher current completes the slew in a proportionally shorter time. This, however, has net power savings as the amplifier now needs a lower gm, with more time made available for the settling. To increase the time 't' available for settling the bias currents in the slew phase are made four times the current used in the settling phase. The disturbance in the bias lines caused due to 4:1 scaling of currents has enough time to settle out completely.

Another substantial power savings can be found by considering the amplifier demands in phase 1, where the second stage samples the output of the first stage. In this phase amplifier non-idealities only affect the integration results which are negligible when input referred. Hence, bias currents in this phase can be reduced to one fourth the bias currents in the settling phase. This level was chosen to assure that adequate time was made available for settling of the chopping artefacts, second integrator sampling of the amplifier and amplifier bias changes. Estimated power savings in this phase are at 30%.[5]

5. Decimation Filter

A multi-function digital filter utilizing a low-power signal processing architecture is used to achieve efficient filtering and decimation of the data coming from a single bit ΔΣ modulator as described earlier. As shown in Figure 6, this filter chip includes integrated peripherals to simplify system design: a low-jitter PLL for standard clock or Manchester inputs, offset and gain calibration and corrections, a test DAC bit stream generator, a time break controller, and eight general purpose I/O pins.[2] The internal structure of the digital filter is shown in Figure 7. Digital filter coefficients for the FIR and IIR filters are included on-chip for a simple setup, or they can be programmed for custom applications. Selectable digital filter decimation ratios produce output word rates from 4000 SPS to 1 SPS, resulting in measurement bandwidths ranging from 1600 Hz down to 400mHz when using the on-chip coefficient sets.

5.1 SINC Filter

The SINC filter's primary purpose is to attenuate out-of-band noise components from the ΔΣ modulators. While doing so, it decimates 1-bit ΔΣ data into lower frequency 24-bit data suitable for the FIR and IIR filters. The SINC filter has three cascaded sections, SINC1, SINC2, and SINC3, which are each made up of the smaller stages. The selected output word rate automatically determines the coefficients and decimation ratios selected for the SINC filters.

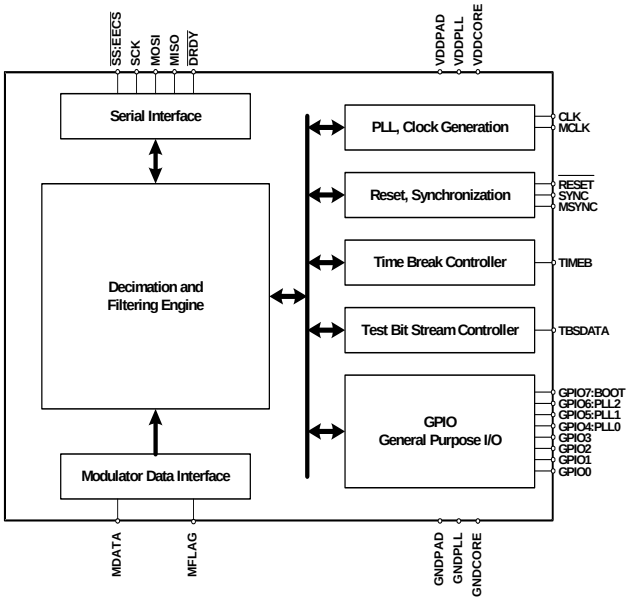

Figure 6 Decimation filter chip block diagram

5.2 FIR Filter

The finite impulse response (FIR) filter block consists of two cascaded stages, FIR1 and FIR2. It compensates for SINC filter droop and creates a low-pass corner to block aliased components of the input signal. On-chip linear phase or minimum phase coefficients can be selected using a configuration command, or the coefficients can be programmed for a custom filter response.

Two sets of on-chip coefficients, linear phase and minimum phase, are available for FIR1 and FIR2. Performance of the on-chip coefficient sets is very good, with excellent ripple and stop band characteristics. A maximum of 255 + 255 coefficients can be programmed into FIR1 and FIR2 to create a custom filter response. The total number of coefficients for the FIR filter is fundamentally limited by the available computation cycles in the digital filter, which itself is determined by the digital filter clock rate.

5.3 Gain and Offset Correction

The digital filter can apply gain and offset corrections to the measurement data. Also, an offset calibration algorithm can automatically calculate the offset correction value. A gain correction value is written to the GAIN registers (0x21), while an offset correction value is written to the OFFSET register (0x25). When enabled, the offset calibration algorithm will automatically calculate an offset correction value and write it into the OFFSET register.

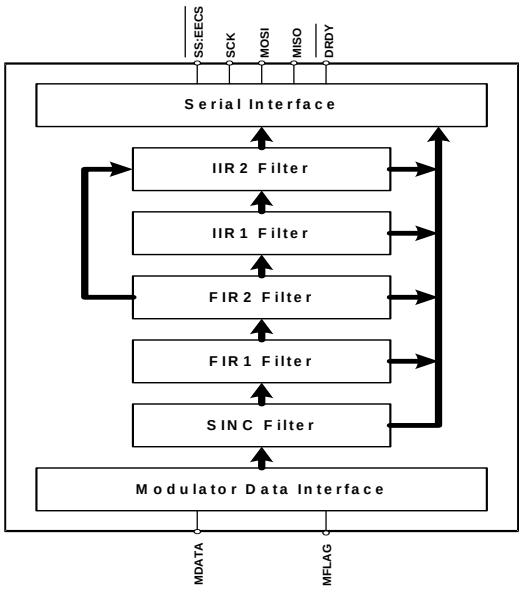

Figure 7 Filter blocks within decimation filter

5.4 Test Bit Stream (TBS)

A digital signal generator built into the digital filter chip produces a 1-bit ΔΣ sine wave or impulse function. This digital test bit stream is connected to the CS4373 test DAC to create high quality analog test signals or internally looped back to the filter MDATA input to test the digital filter and data collection circuitry.

5.5 Synchronization

The MSYNC output signal follows an input to the SYNC pin. The MSYNC signal sets a reference time (time 0) for all operations in the network. The MSYNC phase aligns the modulator sampling instant to guarantee synchronous analog sampling across a measurement network. MSYNC aligns the timings of TBS. The SINC filter is also synchronized to the external system by the MSYNC signal.

6. Self-Test Delta Sigma DAC

A block diagram of the self-test one-bit ΔΣ digital to analog converter (called test DAC) is given in Figure 8. It is a 24 bit DAC driven by one-bit ΔΣ test bit stream (TBS) from the digital filter chip as discussed in the next section. It has been especially designed for seismic application. It produces a differential 118dB linear sinusoidal signal. The frequency and the amplitude are determined by the TBS supplied by the digital filter block. The two sets of differential analog outputs, one precision and the second one buffered, simplifies the seismic data acquisition system calibration and sensor testing. Both outputs have binary weighted high precision attenuator ranging 1, ½,---to 1/64. [3]

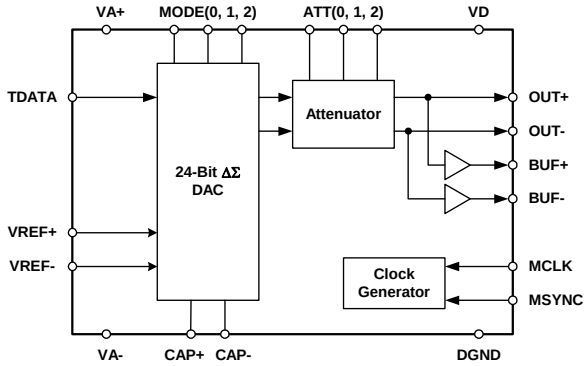

Figure 8 Block diagram of the self-test ΔΣ DAC

The principle of low distortion ΔΣ ADC is used to implement a low distortion DAC.[7] The first integrator of ΔΣ ADC has one continuous time input voltage and the second input is a digital data bit stream. In an ADC the input is continuous time signal and the feedback and output is single bit data. In this DAC design, the same block is used where the input is a single-bit data and the output and the feedback is a continuous time signal. The detailed architecture is given in Figure 9.

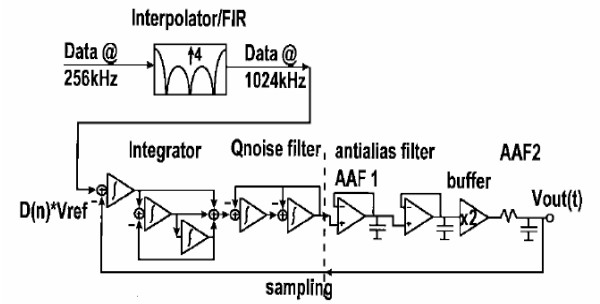

Figure 9 Architecture of self-test ΔΣ DAC

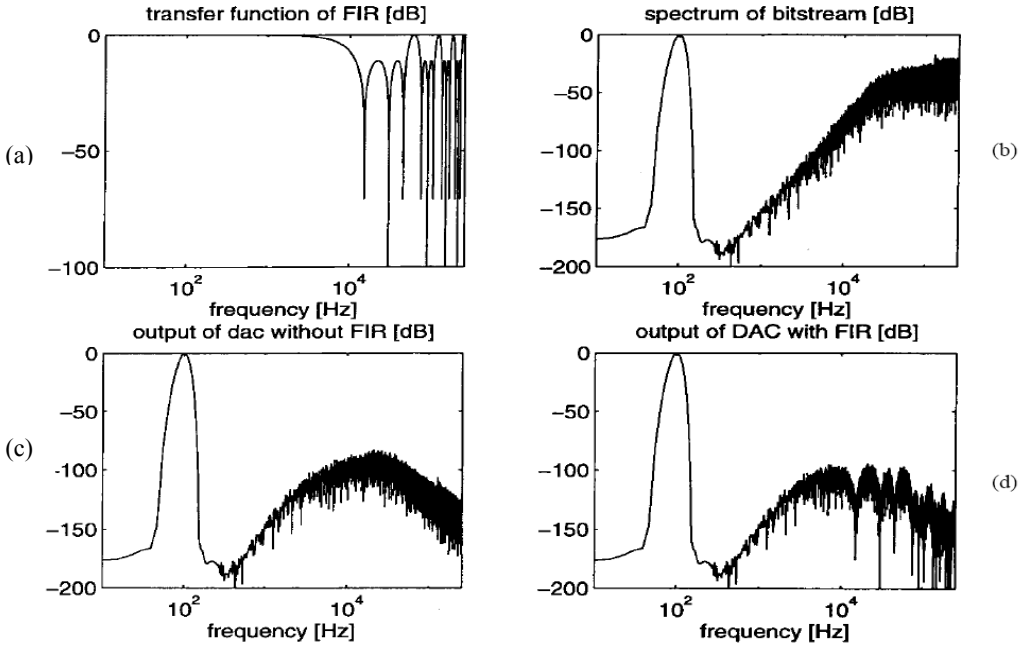

Figure 10 (a) Transfer function of FIR filter,
(b) wide-band power spectrum of TBS
(c) Output of DAC without FIR filter
(d) Output of DAC with FIR filter

Although the system looks complex, all but the first integrator is non-critical. The first integrator is the same as in the ADC described in the previous section. It has dynamic biasing to save power.

The TBS is generated using a fourth order ΔΣ modulator in the digital filter chip. The quantization noise increases at 400Hz. The incoming TBS has a 256k bit rate and the sampling in the DAC is done at 1024kSPS. This difference is utilized to implement an interleaved FIR filter. The filtering reduces the out of band quantization noise in the DAC. The transfer function of the FIR filter, wide band spectrum of TBS, wide-band spectrum of DAC before and after FIR filter is shown in Figure 10. There is a 10dB attenuation of the out-of-band noise due to FIR filtering. [7]

7. Total System Performance in Self-Test Mode

Ten boards, each containing four data acquisition channels, were tested at 25°C, -40°C and 85°C. Each channel was tested using its associated self-test DAC. Two channels (CH1 and CH2) of each board had geophone amplifiers (CS3301) and the two channels (CH3 and CH4) had hydrophone amplifiers (CS3302). These boards had PGIAs, ADCs, Decimation Filters and Self-Test DACs which had been tested under production test programs to meet the specifications given in their respective data sheets [2]. The average linearity of each channel is given in table 1.

Table 1 Total System Performance in Self-Test Mode

	Linearity in dB		
Channels	25°C	-40°C	85°C
CH1	115.66	112.63	114.26
CH2	114.60	113.53	113.69
CH3	113.40	112.64	112.89
CH4	114.15	112.05	112.74

The average linearity across temperature was higher than 112dB at 5volts peak to peak differential signal level and 31.25Hz test frequency. The average power consumption per channel was less than 105mW at 5 volts power supply. The data acquisition system presented is especially designed for seismic exploration; however, it is very flexible to be useful in many other low-frequency high-precision low power applications.

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