Technical Note

Using Micron® MT29F2G08AACWP NAND Flash Memory In Toshiba TC58NVG1S3BTG00 Applications

For functional and parametric specifications, refer to the product data sheet on Micron's Web site:
www.micron.com/products/nand

Introduction

Micron offers a family of NAND Flash devices that target high-density, low-cost applications. This technical note compares the third-generation 2Gb Micron® NAND Flash device with 2Gb Toshiba device TC58NVG1S3BTG00.

In most instances throughout this technical note, the actual Micron and Toshiba specifications appear together. Differences between the two specifications are pointed out and implications discussed in the applicable section of the document. Where a difference is of particular importance to the user, pertinent details are highlighted. Where no difference exists between the two specifications, this is noted as well.

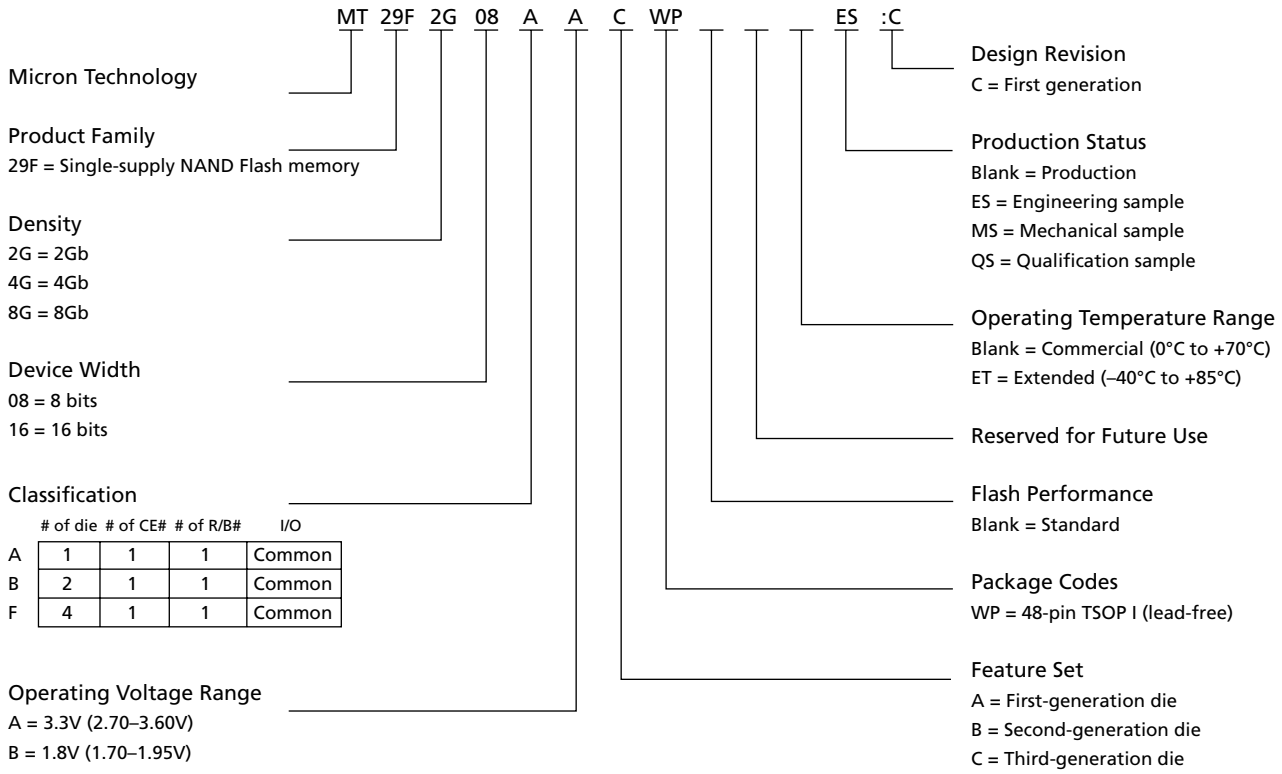
Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications. All information discussed herein is provided on an "as is" basis, without warranties of any kind.

Part Numbering

Figure 1 shows how to interpret the Micron part numbers, as well as supported options.

Figure 1: Micron NAND Flash Part Number Chart



	# of die	# of CE#	# of R/B#	I/O
A	1	1	1	Common
B	2	1	1	Common
F	4	1	1	Common

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Part Replacement

Micron NAND Flash devices offer a replacement for Toshiba parts. Table 1 provides equivalent part numbers.

Table 1: Micron and Toshiba Equivalent Parts

Micron Part	Toshiba Part	Density	Voltage	Bus Width	Device ID	Package Type	Replacement Instructions
MT29F2G08AACWP (single 2Gb die)	TC58NVG1S3BTG00 (dual 1Gb-die stack)	2Gb	3.3V	8	DAh	48-pin TSOP Type 1	Direct replacement

Architecture: Valid Blocks

Micron and Toshiba specifications are identical with respect to the number of valid blocks in the devices. Table 2 provides a side-by-side comparison.

Table 2: Valid Block Comparison

Parameter	Symbol	Micron				Toshiba			
		Min	Typ	Max	Unit	Min	Typ	Max	Unit
Number of valid blocks	N_{VB}	2,008	–	2,048	blocks	2,008	–	2,048	blocks

Hardware Compatibility

In addition to providing replacements for Toshiba devices, Micron NAND Flash devices offer specifications that are more suitable for current designs.

DC Operating Conditions

The Micron NAND Flash specification is basically the same as the Toshiba specification (see Table 3); however, Micron and numerous other manufacturers have moved away from using the older TTL specification designated by Toshiba. Most current designs are CMOS, where a ratio (V_{CC} × 0.8) for the V_{IH} parameter and (V_{CC} × 0.2)for V_{IL} is more appropriate.

The published Micron V_{IH} specification is 80 percent of V_{CC}. This is a subtle but important parameter difference. In lower-voltage systems, the old TTL specification is meaningless, as V_{CC} values can be less than the Toshiba V_{IH} specification.

Table 3: Recommended DC Operating Conditions

Parameter	Symbol	Micron				Toshiba			
		Min	Typ	Max	Unit	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	2.7	3.3	3.6	V	2.7	3.3	3.6	V
High-level input voltage	V_{IH}	V_{CC} × 0.8	–	V_{CC} + 0.3	V	2.0	–	V_{CC} + 0.3	V
Low-level Input voltage	V_{IL}	–0.3	–	V_{CC} × 0.2	V	–0.3[1]	–	0.8	V

Notes: 1. Toshiba device: –2V (pulse with less than 20ns).

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

DC Operating Characteristics

Micron and Toshiba DC operating characteristics are shown in Table 4.

Table 4: DC Characteristics
T_A = 0 to 70°C; V_{CC} = 2.7–3.6V

Parameter	Condition	Micron					Toshiba				
		Symbol	Min	Typ	Max	Unit	Symbol	Min	Typ	Max	Unit
Read current	CE# = V_{IL}; I_{OUT} = 0mA; ^tCYCLE = 50ns	I_{CC1}	–	15	30	mA	I_{CC01}	–	10	30	mA
Program current	–	I_{CC2}	–	15	30	mA	I_{CC07}	–	10	30	mA
Erase current	–	I_{CC3}	–	15	30	mA	I_{CC08}	–	10	30	mA
Standby current TTL	CE# = V_{IH}; WP# = 0V/V_{CC}	I_{SB1}	–	–	1	µA	I_{CCS1}	–	–	1	µA
Standby current CMOS	CE# = V_{CC} – 0.2V; WP# = 0V/V_{CC}	I_{SB2}	–	–	50	µA	I_{CCS2}	–	10	50	µA
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	I_{LI}	–	–	±10	µA
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA	I_{LO}	–	–	±10	µA
R/B# output current	V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	–	mA	I_{OL} (R/B#)	–	8	–	mA
High-level output voltage	V_{CC}, I_{OH} = –400µA	V_{OH}	2.4	–	–	V	V_{OH}	2.4	–	–	V
Low-level output voltage	V_{CC}, I_{OL} = 2.1mA	V_{OL}	–	–	0.4	V	V_{OL}	–	–	0.4	V

AC Operating Characteristics

As shown in Figures 2 and 3 on page 5 and Table 5 on page 6, there are slight timing differences between the Micron and Toshiba device specifications. The Toshiba device has a shorter setup time but requires a longer hold time.

These timing differences result from the way Micron and Toshiba define timing parameters. In Figure 3 on page 5, many of Toshiba's setup measurements are tied to the falling edge of WE# (WE# going LOW), while the hold measurements are tied to the rising edge of WE#.

To make it easier for system designers, Micron specifications tie all timing to the rising (active) edge of WE# (see Figure 2 on page 5). Considering only published Toshiba setup and hold times, the Toshiba part appears faster. However, careful examination of the Toshiba specification shows that for the Toshiba device, the system designer must add the setup time (^tCS, for example) to the clock width time (^tWP) to arrive at the actual setup time required before the clock rising edge. In this example, ^tCS = 0ns; add this time to ^tWP = 25ns. The result is 25ns total setup time for the Toshiba device. The total Micron ^tCS specification time is 15ns. Hold time for the Micron device is only 5ns, whereas the Toshiba device requires a 10ns hold time. In all cases, the Micron specification meets or exceeds (is faster than) the Toshiba specification.

The Micron device also runs with faster READ and WRITE clocks, making the Micron device significantly faster.

Designers should take these timing differences into account as they develop designs using either or both devices.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Figure 2: Micron Timing Example

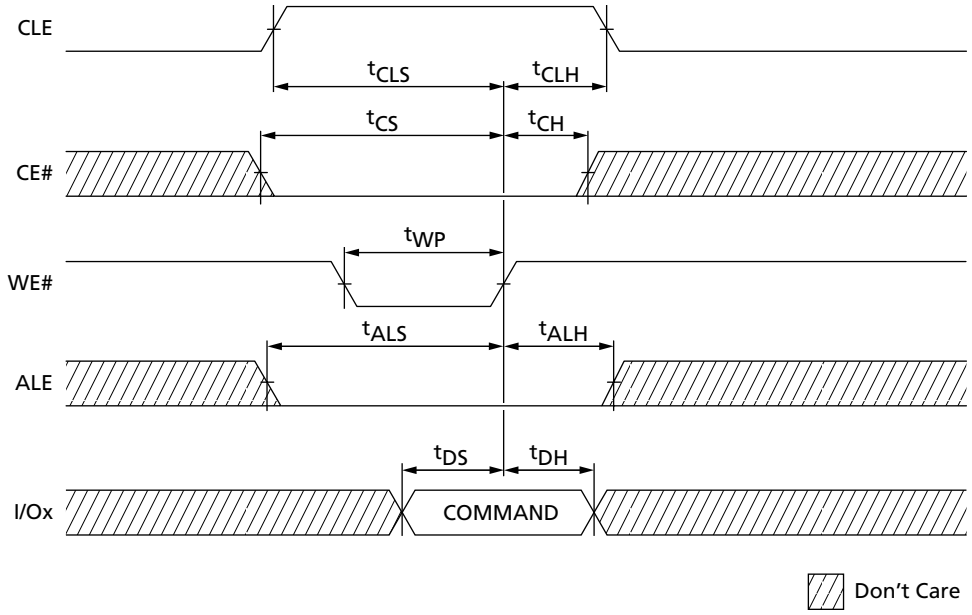
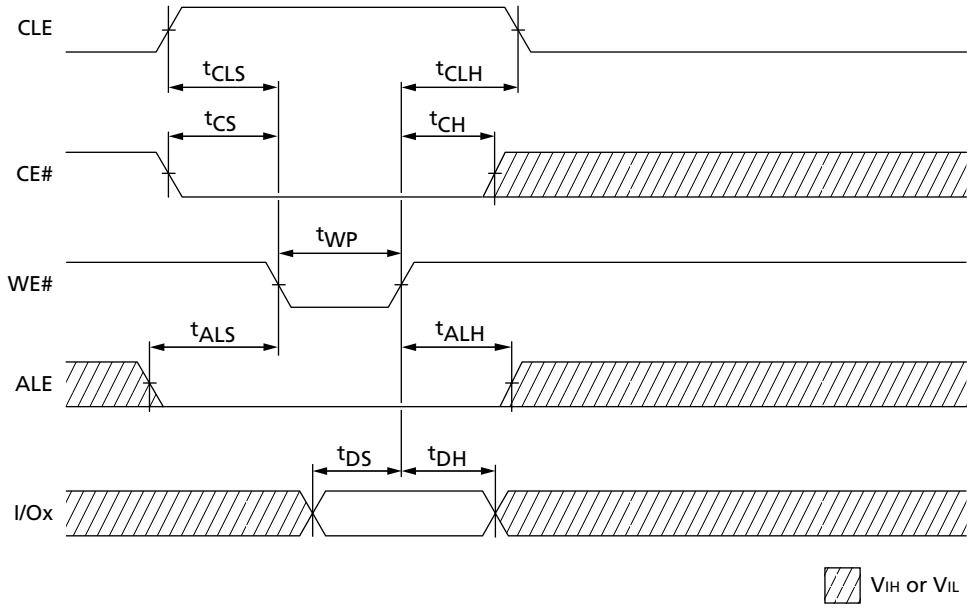


Figure 3: Toshiba Timing Example



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Table 5: AC Characteristics and Recommended Operating Conditions

PARAMETER	Symbol	Micron			Toshiba			Notes
		Min	Max	Unit	Min	Max	Unit	
ALE access time	^{t}ALEA	–	28	ns	–	45	ns	1
ALE hold time	^{t}ALH	5	–	ns	10	–	ns	
ALE setup time	^{t}ALS	10	–	ns	0	–	ns	
CE# access time	^{t}CEA	–	23	ns	–	45	ns	
CE# hold time	^{t}CH	5	–	ns	10	–	ns	
CE# HIGH to output high impedance	^{t}CHZ	–	20	ns	–	20	ns	
CLE access time	^{t}CLEA	–	23	ns	–	45	ns	
CLE hold time	^{t}CLH	5	–	ns	10	–	ns	
CLE setup time	^{t}CLS	10	–	ns	0	–	ns	
CLE access time (READ STATUS)	^{t}CLSTO	–	41	ns	–	45	ns	2
CE# setup time	^{t}CS	15	–	ns	0	–	ns	
CE# HIGH access time (READ STATUS)	^{t}CSTO	–	23	ns	–	45	ns	
Data hold time	^{t}DH	5	–	ns	10	–	ns	
Data setup time	^{t}DS	10	–	ns	20	–	ns	
Output high impedance to RE# falling edge	^{t}IR	0	–	ns	0	–	ns	
Data output hold time	^{t}OH	15	–	ns	10	–	ns	
Memory cell array to starting address	^{t}R	–	25	µs	–	25	µs	
Read cycle time	^{t}RC	30	–	ns	50	–	ns	
RE# access time (serial data access)	^{t}REA	–	18	ns	–	35	ns	
RE# access time (READ ID)	^{t}REAID	–	18	ns	–	35	ns	3
RE# HIGH hold time	^{t}REH	10	–	ns	15	–	ns	
RE# HIGH to WE# LOW	^{t}RHW	30[4]	–	ns	30	–	ns	
RE# HIGH to output high impedance	^{t}RHZ	–	30	ns	–	30	ns	
Read pulse width	^{t}RP	15	–	ns	35	–	ns	
Ready to RE# falling edge	^{t}RR	20	–	ns	20	–	ns	
Device reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	–	6/10/500	µs	
RE# LOW access time (READ STATUS)	^{t}RSTO	–	18	ns	–	35	ns	
Ready to WE# falling edge	^{t}RW	20	–	ns	20	–	ns	
WE# HIGH to busy	^{t}WB	–	100	ns	–	200	ns	
Write cycle time	^{t}WC	30	–	ns	50	–	ns	
WE# HIGH hold time	^{t}WH	10	–	ns	15	–	ns	
WE# HIGH to CE# LOW	^{t}WHC	30[4]	–	ns	30	–	ns	
WE# HIGH to RE# LOW	^{t}WHR	60	–	ns	30	–	ns	
Write pulse width	^{t}WP	15	–	ns	25	–	ns	
WP# HIGH to WE# LOW	^{t}WW	100	–	ns	100	–	ns	4

Notes:
1. The equivalent of Toshiba ^{t}ALEA for the Micron device is the combination of ^{t}AR (10ns) and ^{t}REA (18ns).
2. The equivalent of Toshiba ^{t}CLSTO for the Micron device is the combination of ^{t}CLEA (23ns) and ^{t}REA (18ns).
3. Micron does not distinguish between ID read and data read; ^{t}REA is used for both.
4. The Micron specification does not include this parameter; however, this timing has been verified in lab tests.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

AC Test Conditions

As shown in Table 6, the specifications for the Micron and Toshiba parts are not identical for AC test conditions. The Micron input and output comparison points are presented as a ratio of the VCC voltage.

Table 6: AC Test Conditions

Parameter	Micron	Toshiba
Input level	3.3V, 0.0V	2.4V, 0.4V
Input pulse rise and fall time	5ns	3ns
Input comparison level	Vcc/2	1.5V, 1.5V
Output data comparison level	Vcc/2	1.5V, 1.5V
Output load	C_L (100pF) + TTL	C_L (100pF) + TTL

PROGRAM and ERASE Characteristics

The maximum PROGRAM and ERASE specifications for the Micron and Toshiba devices differ, as shown in Table 7.

Table 7: PROGRAM and ERASE Characteristics
T_A = 0–70°C; Vcc = 2.7–3.6V

Parameter	Symbol	Micron				Toshiba			
		Min	Typ	Max	Unit	Min	Typ	Max	Unit
Number of PROGRAM cycles on same page before ERASE required (per 512 + 16 bytes)[1]	N	–	–	8		–	–	8	
BLOCK ERASE time	^{t}BERASE	–	2	3	ms	–	1.5	10	ms
Average PROGRAM time	^{t}PROG	–	300	700	µs	–	200	500	µs

Notes: 1. The Micron specification is 8 program cycles for each 2,112-byte page.

Absolute Maximum Ratings

Table 8: Absolute Maximum Values Comparison

Rating	Symbol	Micron		Toshiba	
		Value	Unit	Value	Unit
Power supply voltage	VCC	–0.6 to 4.6	V	–0.6 to 4.6	V
Input voltage	VIN	–0.6 to 4.6	V	–0.6 to 4.6	V
I/O voltage	VIO	–0.6 to 4.6	V	–0.6 to (VCC + 0.3V), where (VCC + 0.3V) ≤ 4.6V	V
Power dissipation	PD	< 0.3	W	0.3	W
Soldering temperature (10s)	TSOLDER	260	°C	260	°C
Storage temperature	TSTG	–65 to +150	°C	–55 to +150	°C
Operating temperature	TOPR	0 to 70	°C	0 to 70	°C

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Pin Configuration

With a few noted exceptions, the Micron and Toshiba devices are compatible. Three Micron pins are different from those in the Toshiba device. Comparing the two devices, the I/O pinout is identical; the I/O numbering scheme is different. Micron counts I/O[7:0], and Toshiba uses I/O[8:1].

Micron Pin 6 on the 2Gb Device

This pin is NC on the 2Gb Micron device and is connected to ground on the Toshiba device. Grounding pin 6 on the Micron device is a suitable option.

Micron Pins 6 and 10 on the 8Gb Device

On the 8Gb Micron device, pins 6 and 10 are used as the second ready/busy (R/B#) and chip enable (CE#) signals. Designers interested in larger capacities should connect pins 6 and 10 to a second channel of their controller. These pins are NC on both the Micron and the Toshiba 2Gb devices.

Forward-thinking designers should be aware of the additional capabilities of Micron's larger devices and orient their designs to take full advantage of these capabilities in future product generations.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Figure 4: Micron Pin Configuration (x8)

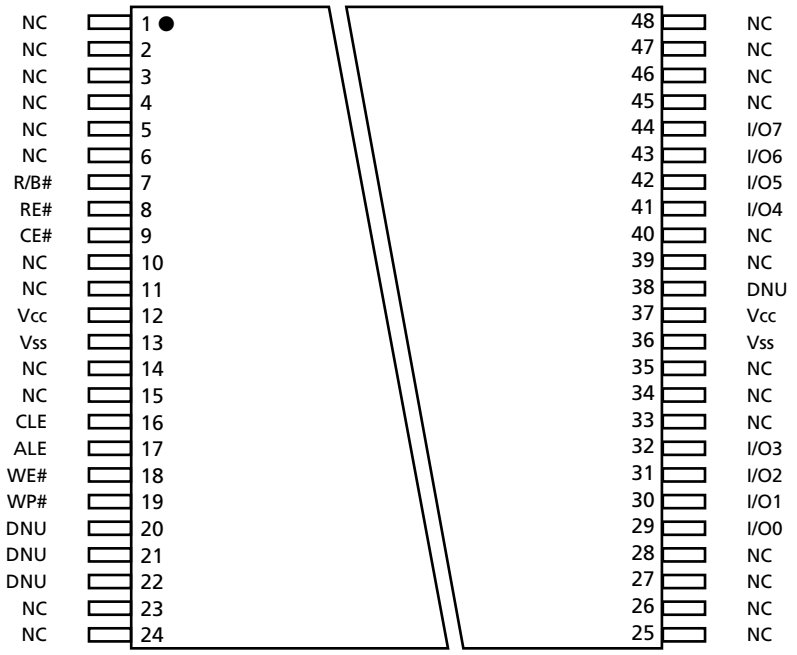
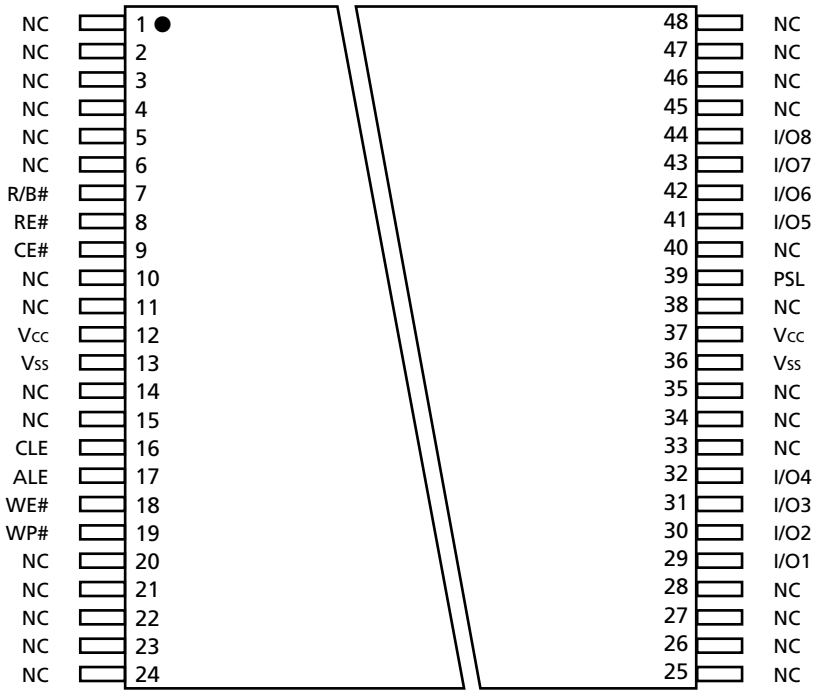


Figure 5: Toshiba Pin Configuration (x8)



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Power-Up

The Micron and Toshiba devices use the same supply voltage and power-on threshold (2.5V). It is important to note that the Toshiba device can take up to 1ms to become ready, whereas the Micron device is ready in 100µs. In a mixed environment, the Micron device will report a ready status earlier than the Toshiba device without compromising Toshiba parts.

Figure 6: Micron Power-Up

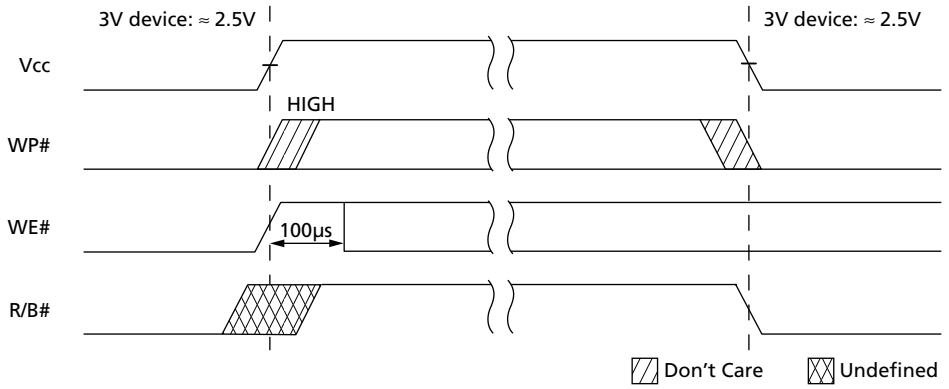
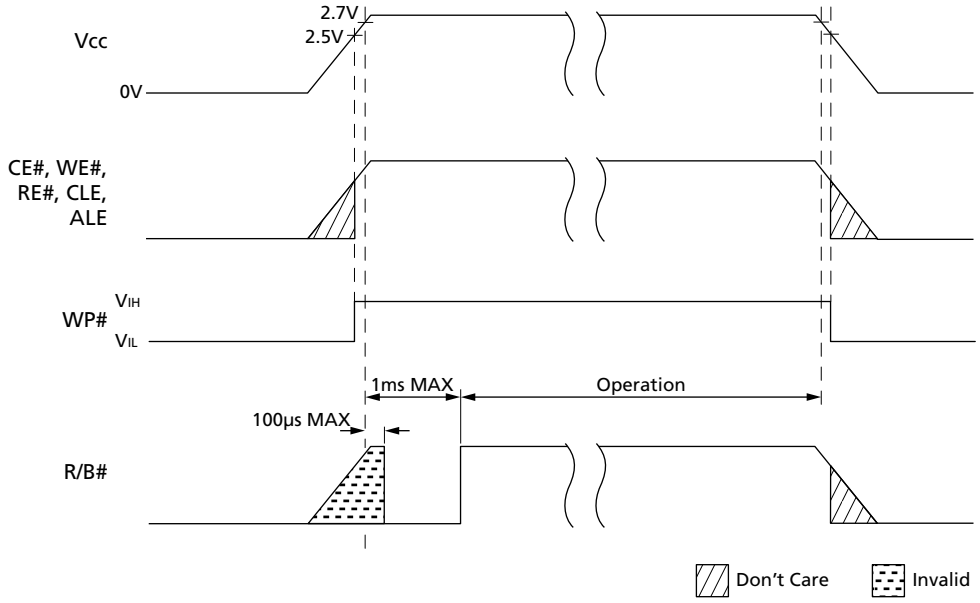


Figure 7: Toshiba Power-Up



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Bus Operations

The Micron device offers compatibility with all Toshiba bus operations. Tables 9 and 10 demonstrate this compatibility.

Table 9: Micron Logic Table

		CLE[1]	ALE	CE#	WE#	RE#	WP#
Read mode	Command input	H	L	L	↑	H	X
	Address input	L	H	L	↑	H	X
Write mode	Command input	H	L	L	↑	H	H
	Address input	L	H	L	↑	H	H
Data input		L	L	L	↑	H	H
Sequential read and data output		L	L	L	H	↓	X
During READ (busy)		L	L	L	H	H	X
During PROGRAM (busy)		X	X	X	X	X	H
During ERASE (busy)		X	X	X	X	X	H
Write protect		X	X	X	X	X	L
Standby		X	X	H	X	X	0V/Vcc[2]

Notes: 1. Mode selection settings: H = Logic level HIGH; L = Logic level LOW; X = "Don't care."
2. WP# should be biased to CMOS HIGH or LOW for standby.

Table 10: Toshiba Logic Table

	CLE[1]	ALE	CE#	WE#	RE#	WP#
Command input	H	L	L	↑	H	X
Data input	L	L	L	↑	H	H
Address input	L	H	L	↑	H	X
Serial data output	L	L	L	H	↓	X
During PROGRAM (busy)	X	X	X	X	X	H
During ERASE (busy)	X	X	H	X	X	H
During READ (busy)	X	X	L	H	H	X
PROGRAM, ERASE inhibit	X	X	X	X	X	L
Standby	X	X	H	X	X	0V/Vcc

Notes: 1. Mode selection settings: H = Logic level HIGH; L = Logic level LOW; X = "Don't care."

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Software

Software Compatibility

The most important consideration relative to software compatibility is to ensure that multiple device IDs are supported by the intended software. This will make it easier to meet design requirements for NAND Flash devices from multiple vendors.

Micron NAND Flash software has a number of modules to aid system development processes. To learn about Micron NAND Flash software, contact a local Micron sales office.

As discussed previously, the Micron device supports additional commands that the Toshiba device does not. This will not present a problem, as the Micron device is backward-compatible with the Toshiba device. When these additional commands are implemented, additional performance gains may be realized without incurring additional hardware costs.

Software Support for Device IDs

All NAND Flash devices support a READ ID command to report each device ID (device manufacturer and device configuration). Most controllers utilize this feature to identify and correctly support the features of a specific device. For Toshiba devices, the first two device ID bytes reported are 98h and DAh (see Figure 9 on page 13). For Micron devices, the first two device ID bytes reported are 2Ch and DAh (see Figure 8 on page 13).

If the user device ID software interrogates bytes 3 and 4 of the Toshiba device, the software will require minor modification in order to utilize the data reported from these bytes on Micron devices.

Table 11: Byte Allocation

Byte	Description	Micron	Toshiba
First	Manufacturer ID	2Ch	98h
Second	Device ID	See Table 1 on page 3	See Table 1 on page 3
Third	Chip #, cell type, program page, write cache	80h	81h or 01h
Fourth	Organization: x8	95h	15h
	Organization: x16	D5h	NA
Fifth	Plane #, plane size	NA	44h or C4h

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Figure 8: Micron READ ID Timing

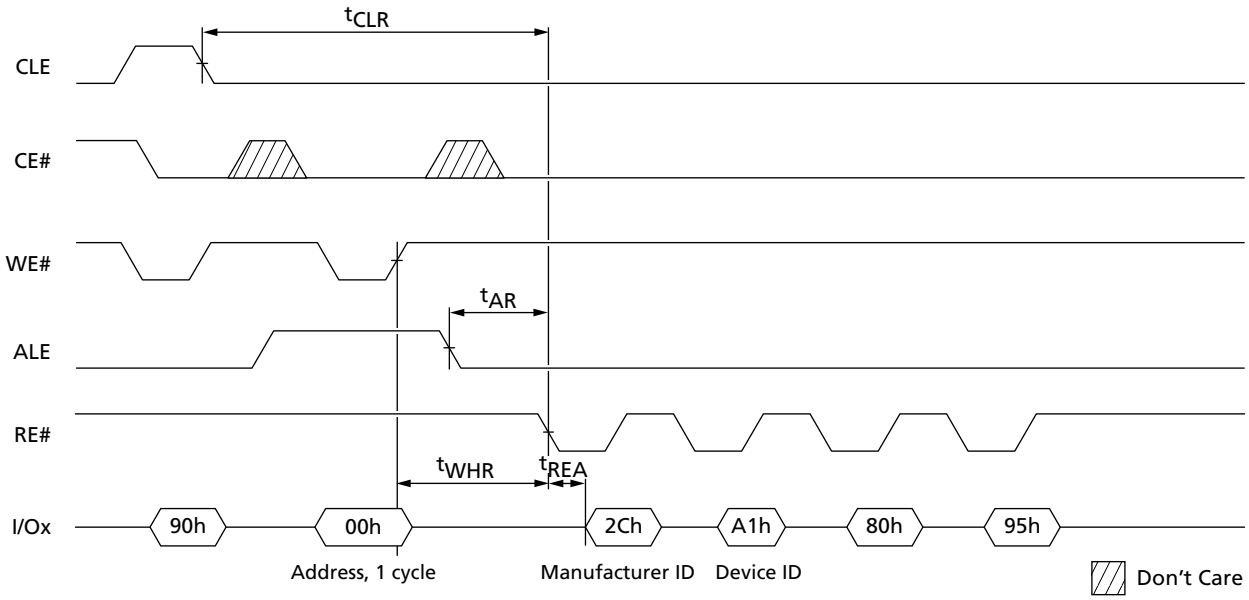
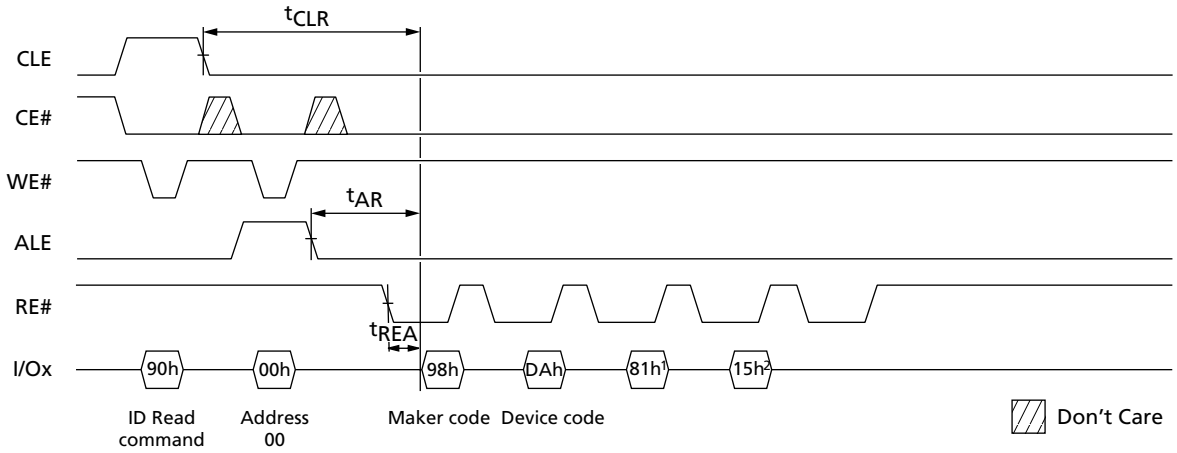


Figure 9: Toshiba ID Read Timing



Notes: 1. 81h or 01h
2. 95h or 15h
3. For ^{t}REAID and ^{t}ALE access time specifications, refer to Table 5 on page 6.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Commands

Table 12 shows the command set for the Micron NAND Flash device, and Table 13 shows the commands for the Toshiba device. While these two tables appear to be significantly different, the Micron device provides a superset of the Toshiba commands, thus offering compatibility. The primary difference is in the way commands are specified for the devices.

Figures 10 and 11 on page 15 show READ operation timing for the Micron and Toshiba devices, respectively. It is important to note the additional new performance-enhancing commands on the Micron device. Full explanation of these additional command options exceeds the scope of this document. Contact a local Micron sales office for details.

Table 12: Micron Command Set

Operation (Command)	Cycle 1	Cycle 2	Valid During Busy
PAGE READ	00h	30h	No
PAGE READ CACHE MODE START	31h	–	No
PAGE READ CACHE MODE START LAST	3Fh	–	No
READ for INTERNAL DATA MOVE	00h	35h	No
RANDOM DATA READ	05h	E0h	No
READ ID	90h	–	No
READ STATUS	70h	–	Yes
PROGRAM PAGE	80h	10h	No
PROGRAM PAGE CACHE MODE	80h	15h	No
PROGRAM for INTERNAL DATA MOVE	85h	10h	No
RANDOM DATA INPUT for PROGRAM	85h	–	No
BLOCK ERASE	60h	D0h	No
RESET	FFh	–	Yes

Table 13: Toshiba Command Set

Command	First Cycle	Second Cycle	Acceptable While Busy
Serial Data Input	80h	–	
Read	00h	30h	
Column Address Change in Serial Data Output	05h	E0h	
Auto Page Program	80h	10h	
Read Address Input	00h	–	
Column Address Change in Serial Data Input	85h	–	
Auto Block Erase	60h	D0h	
ID Read	90h	–	
Status Read	70h	–	No
Reset	FFh		No

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Figure 10: Micron READ Timing

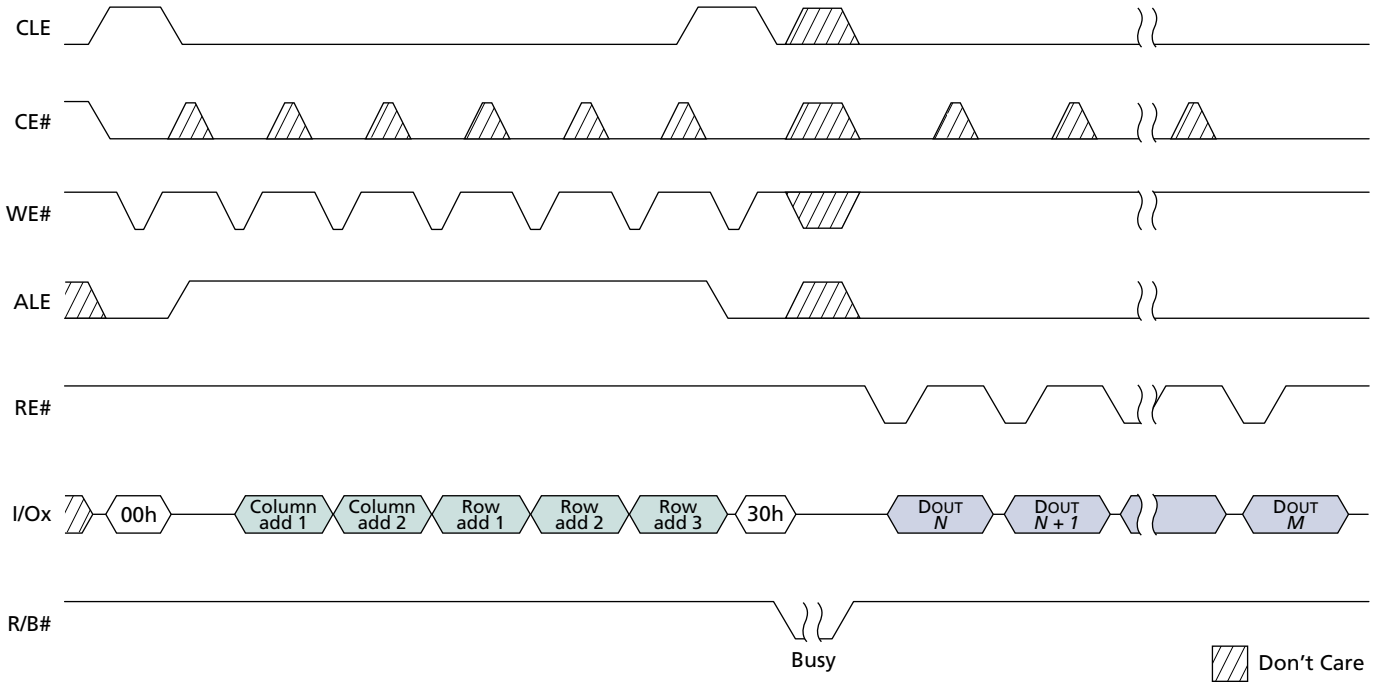
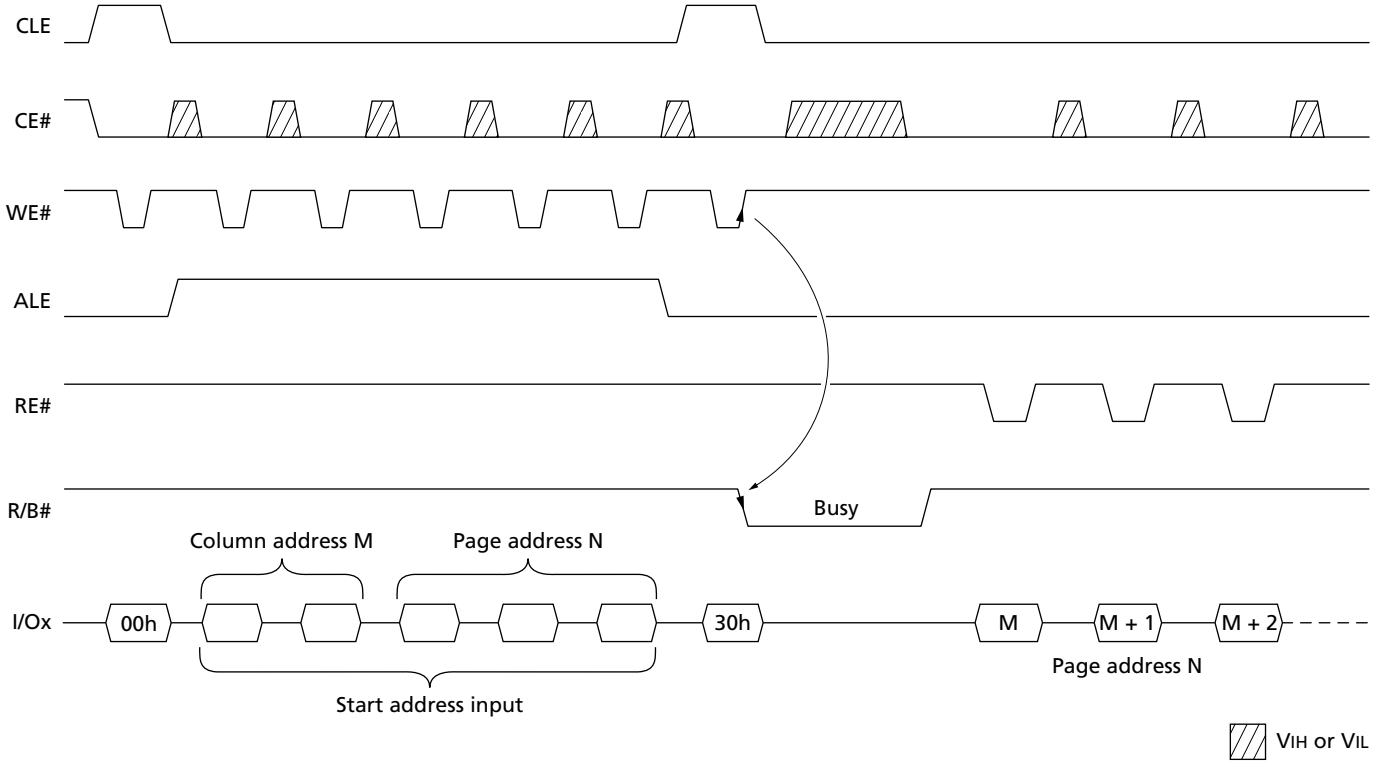


Figure 11: Toshiba READ Timing



Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Addressing

Address maps for the Micron and Toshiba parts, Tables 14 and 15, respectively, demonstrate consistent mapping between the two parts. Only the naming conventions differ.

In the Toshiba device, the column addresses (CA) and page addresses (PA) are numbered separately, while Micron provides separate numbering between the column addresses (CA), page addresses (PA), and block addresses (BA).

Table 14: Micron Address Map

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA16

Table 15: Toshiba Address Map

Cycle	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	L	L	L	L	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
Fifth	L	L	L	L	L	L	L	PA16

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Status Register

The status register (SR) bit formats for the Micron and Toshiba devices are consistent.

Table 16: Micron Status Register Bit Format

SR Bit	PROGRAM PAGE	PROGRAM PAGE CACHE MODE	PAGE READ	PAGE READ CACHE MODE	BLOCK ERASE	Definition
0	Pass/fail	Pass/fail (N)	–	–	Pass/fail	0 = Successful PROGRAM/ERASE 1 = Error in PROGRAM/ERASE
1	–	Pass/fail (N-1)	–	–	–	0 = Successful PROGRAM/ERASE 1 = Error in PROGRAM/ERASE
2	–	–	–	–	–	0
3	–	–	–	–	–	0
4	–	–	–	–	–	0
5	Ready/busy	Ready/busy[1]	Ready/busy	Ready/busy[1]	Ready/busy	0 = Busy 1 = Ready
6	Ready/busy	Ready/busy cache[2]	Ready/busy	Ready/busy cache[2]	Ready/busy	0 = Busy 1 = Ready
7	Write protect	Write protect	Write protect	Write protect	Write protect	0 = Protected 1 = Not protected

Notes: 1. Status register bit 5 is "0" during the actual programming operation. If cache mode is used, this bit will be "1" when all internal operations are complete.
2. Status register bit 6 is "1" when the cache is ready to accept new data. R/B# follows the state of bit 6.

Table 17: Toshiba Status Register Bit Format

	Status	Output	
I/O1	Chip status 1	Pass: 0	Fail: 1
I/O2	Not used	Invalid	Invalid
I/O3	Not used	0	
I/O4	Not used	0	
I/O5	Not used	0	
I/O6	Ready/busy	Ready: 1	Busy: 0
I/O7	Ready/busy	Ready: 1	Busy: 0
I/O8	Write protect	Protect: 0	Not protected: 1

Note: The pass/fail status on I/O1 and I/O2 is valid only when the device is in the ready state.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Summary

The Micron MT29F2G08AACWP NAND Flash device provides a replacement for the Toshiba TC58NVG1S3BTG00 device, with compatible pinout and hardware configurations. Minor differences in the ID and status registers are readily addressed using controller firmware to support applications where the Micron device will be used alone or in combination with other manufacturers' devices.

References

The production data sheet for the 2Gb Micron NAND Flash MT29F2G08AACWP device, dated 12/2006, and the Toshiba TC58NVG1S3BTG00 NAND Flash device data sheet, dated 2004-08-20A (38 pages), were used to prepare this comparative technical note. For functional and parametric specifications, refer to the product data sheet on the Micron Web site at www.micron.com/products/nand/.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992
Micron, the M logo, and the Micron logo are trademarks of Micron Technology, Inc.
All other trademarks are the property of their respective owners.

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Revision History

Rev. B **5/07**

- Removed PRE throughout document.
- Updated Micron part number from MT29F2G08AABWP to MT29F2G08AACWP and Toshiba part number from TH58NVG1S3AFT05 to TC58NVG1S3BTG00 throughout.
- Updated Web links and styles; inserted page 1 link in "References" on page 18.
- Revised compatibility language throughout.
- "Introduction" on page 1: Revised description.
- Figure 1 on page 2: Updated diagram.
- "DC Operating Conditions" on page 3: Added reference to V_{IL} parameter ratio.
- Table 1 on page 3: Updated table, deleted TC58NVG1S3AFT5 (single 2Gb die); deleted note.
- Table 3 on page 3: Changed Micron V_{IL} (MAX) to $V_{CC} \times 0.2$.
- "DC Operating Characteristics" and "AC Operating Characteristics" on page 4: Revised description.
- Table 4 on page 4: Changed V_{CC} range from 2.7–3.3V to 2.7–3.6V in subheading. For Toshiba, inserted $I_{CCS}2$ (TYP) value of 10µA, changed typical values $I_{CC}01$, $I_{CC}07$ and $I_{CC}08$ from 15 to 10. Clarified standby current parameters and changed unit for standby current CMOS ($I_{SB}2/I_{CCS}2$) from mA to µA. Updated TYP and MAX currents and added Micron symbols.
- "AC Test Conditions" on page 7: Clarified description.
- "PROGRAM and ERASE Characteristics" on page 7: Clarified description.
- Table 7 on page 7: Changed Toshiba ^{t}BERASE (TYP) to 1.5ms, ^{t}BERASE (MAX) to 10ms, and ^{t}PROG (MAX) to 500µs; clarified number of PROGRAM cycles on same page before ERASE required and changed MAX value for Toshiba N row from 2 to 8.
- Table 8 on page 7: Clarified Toshiba V_{IO} value; changed Micron V_{CC}, V_{IN}, and V_{IO} values from –0.2V to –0.6V.
- Figure 4 on page 9: Deleted x16, changed pins 6 and 10 to "NC," pins 20–22, 38 to "DNU," reformatted diagram, removed notes.
- Figure 5 on page 9: Changed pin 6 to "NC" and pin 39 to "PSL."
- "Power-Up" on page 10: Changed 10µs to 100µs.
- Figure 6 on page 10: Removed 1.8V device reference; changed 10µs to 100µs; updated figure.
- Table 9 on page 11: Changed CLE, ALE, and CE# to LOW and WE# and RE# to HIGH during READ (busy).
- "Bus Operations" on page 11: Revised description.
- Table 10 on page 11: Changed CE# to HIGH during ERASE (busy), CE# to LOW and WE# and RE# to HIGH during READ (busy).
- "Software Compatibility" on page 12: Revised description.
- "Software Support for Device IDs" on page 12: Added cross references.
- Table 11 on page 12: Added table.
- Figure 8 on page 13: Updated figure.
- Figure 9 on page 13: Removed Toshiba device ID byte 5 (44h) from figure and deleted corresponding note; updated figure.
- "Commands" on page 14: Revised description.
- Table 13 on page 14: Added Read and Column Address Change in Serial Data Input commands, removed Read Address Input, Read Start, and Read Column Change, changed Auto Program to Auto Page Program 80h-10h, changed Column Address

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.

Change in Serial Data Output to 05h-E0h, changed Status Read and Reset to not acceptable while busy.

- Table 14 on page 16: Changed third-, fourth-, and fifth-cycle I/O0 address values to PA0–PA5 and BA6–BA16; deleted note.
- Table 15 on page 16: Deleted notes.
- Table 16 on page 17: Removed bits [15:8].
- Table 17 on page 17: Changed I/O2 status to “not used” and output to “invalid,” I/O7 status to “ready/busy.”
- “References” on page 18: Updated data sheet references.

Rev. A 4/05

- Initial release

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2004 Micron Technology, Inc. All rights reserved.