SH7780 Group

Example of Memory-to-Memory Transfer by the DMAC (LRAM to DDR SDRAM)

Introduction

This application note gives an example of how to set products of the SH7780 Group for inter-memory (LRAM to DDR SDRAM) data transfer and describes a sample application for this purpose.

Target Device

SH7780 (MS7780SE03 Solution Engine by Hitachi ULSI Systems)

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1. Preface

1.1 Specifications

DMA channel 0 is used to transfer all data on pages 0 and 1 (16 KB) of the L memory to DDR-SDRAM. Checking to see if the transfer is complete proceeds every 5 ms; if it is complete, DMA transfer is started again.

Cycle-stealing mode is selected as the bus mode and DMA transfers are requested in auto request mode (transfer requests by software).

1.2 Module Used

- DMAC channel 0

1.3 Applicable Conditions

• MCU	SH7780	
• Operating frequency	Internal clock	: 400 MHz
	SuperHyway clock	: 200 MHz
	Peripheral clock	: 33 MHz
	DDR clock	: 160 MHz
	External clock	: 33 MHz
	PCI bus clock	: 33 MHz
• Clock operating mode	Mode 3 (MODE7 = low, MODE2 = low, MODE1 = high, MODE0 = high)	
• Data alignment	Little endian	
• Addressing mode	29-bit	
• C compiler	SuperHRISC Engine Family C/C++ Compiler Package Ver.9.1.0 (manufactured by Renesas Technology)	

1.4 Related Application Notes

The operation of the reference program for this document was confirmed with the setting conditions described in the following application notes.

- SH7780 Initialization Example: REJ06B0712-0100
- Example of TMU Operation (Generating 1 Second by Fixed Interval Timer): REJ06B0718-0100
  Note that the timer unit (TMC channel 0) is used as a fixed-interval timer to measure 5-ms periods in this application note.

Please refer to these application notes in combination with this one.

2. Description of the Sample Application

This sample program uses channel 0 of the direct memory access controller (DMAC) to perform block transfer from the on-chip RAM (LRAM) to external memory (DDR-SDRAM). After the first transfer starts, the completion of transfer is checked every 5 ms; if it is, the program restarts the transfer of next block.

When one-block transfer is complete, the program disables transfer and waits for 5 ms. It waits after the completion of transfer in the same way when an address error has occurred during transfer.

2.1 Description of the Sample Program

This sample program consists of the following four source files.

(1) dmac.c
(2) main.c
(3) intprg.c
(4) vecttbl.src

Since the code for *Example of TMU Operation (Generating 1 Second by Fixed Interval Timer)* is used to count 5-ms intervals, tmu.c from the corresponding sample application should be added to this project.

(1) dmac.c describes the functions used in this program to set up DMAC operation and to restart DMAC transfer when an address error is encountered.
This program code is not included in the application for *SH7780 Initialization Example*, which is used as its basis.

(2) main.c sets the status register (SR) and calls the function to set up DMAC operation.
Change main.c that was included with *SH7780 Initialization Example* as required to match main.c for this sample program.

(3) intprg.c describes the interrupt program called from the exception/interrupt handler.
Change intprg.c that was included with *SH7780 Initialization Example* as required to match intprg.c for this sample program. Since counting of 5-ms intervals is handled in the same way as in *Example of TMU Operation (Generating 1 Second by Fixed Interval Timer)*, intprg.c should also be modified to match that sample program.

(4) vecttbl.src describes the exception/interrupt vector table (including vector-table entries), and interrupt mask table.
To ensure that interrupts that have been accepted are not accepted again while they are being processed, the interrupt mask levels to be set in the IMASK bits of the status register should be described in the interrupt mask table.
Change vecttbl.src that was included with *SH7780 Initialization Example* as required to match vecttbl.src for this sample program. As with intprg.c, to use 5-ms counting as in *Example of TMU Operation (Generating 1 Second by Fixed Interval Timer)*, make modifications to include interrupt mask levels with reference to *Example of TMU Operation (Generating 1 Second by Fixed Interval Timer)*.

2.2 Operational Overview of Module Used

When the DMAC has a DMA transfer request, it initiates transfer in accord with the selected order of priority for its channels, and ends the transfer when the transfer-end condition is satisfied. There are three activation methods for DMA transfer: auto request, external request and peripheral module request. The bus mode can be selected as either burst mode or cycle-stealing mode.

Table 1 gives an overview of the DMAC.

Table 1 DMAC Overview

Item	Overview
No. of channels available	12 (channels 0 to 3 can accept external requests)
Address space	4 Gbytes
Data transfer unit	Byte, word (2 bytes), longword (4 bytes), 16 bytes, and 32 bytes
Maximum transfer count	16777216
Address mode	Dual address mode
Transfer requests	Auto request, external request, and peripheral module request
Bus modes	Cycle-stealing mode and burst mode
Channel priority	Fixed mode and round-robin mode
Interrupt request	An interrupt request is issued to the CPU after a transfer is half completed or completed, and when an address error occurs.
External request detection	The following four senses for DREQ input detection are available: low or high level, or rising or falling edge.
Transfer request acknowledge signal/transfer end signal	Active levels for DACK and DRAK can be set independently.

2.3 Procedure for Setting Module Used

This section describes the initialization procedure for inter-memory transfer by the DMAC. Transfer requests are in auto request mode.

In this program, the following initial settings are made at the beginning of the main function on the assumption that this is based on the program for *SH7780 Initialization Example*. Since operation in privileged mode is a precondition for the program doing this, take care with regard to the processing mode when you adapt this code for use with other programs etc.

Figure 1 shows an example of the initialization sequence for data transfer between the LRAM and DDR SDRAM memory areas. For details on the settings of individual registers, see the *SH7780 Group Hardware Manual*.

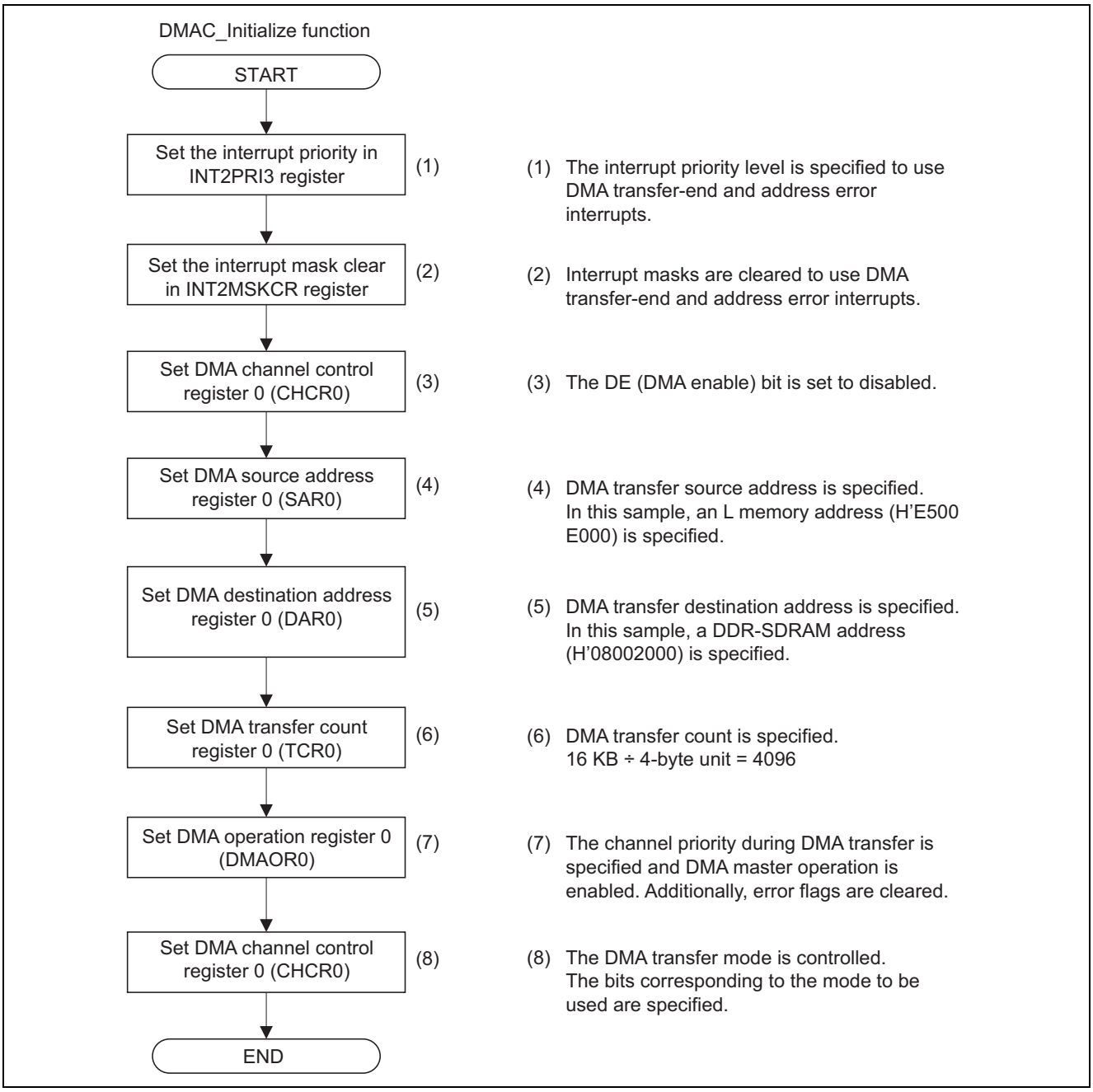


Figure 1 Flow of Setting the DMAC for Inter-Memory Transfer

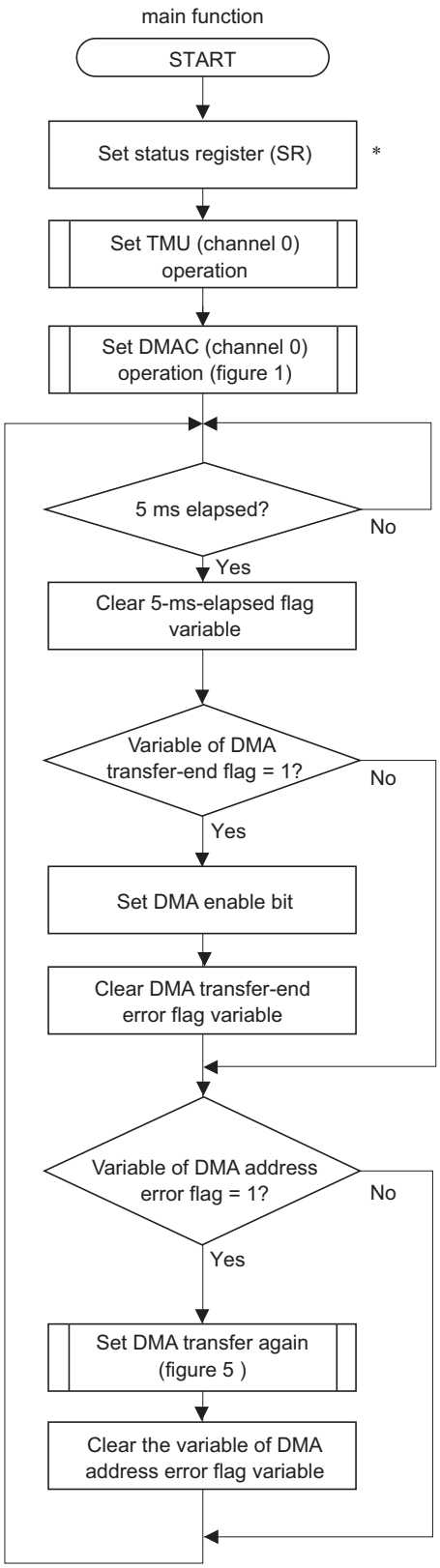
2.4 Procedure for processing the Sample Program

Table 2 gives examples for setting DMAC-related registers.

The following pages provide sample flowcharts of the main function, transfer-end interrupt handling, address-error interrupt handling, and restarting transfers.

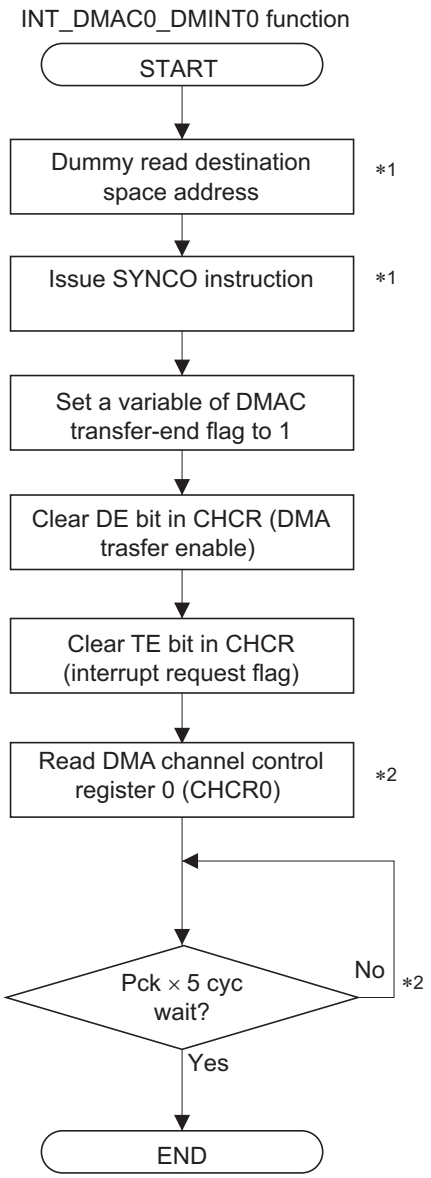
Table 2 DMAC Setting

Register Name	Address	Setting	Description
Interrupt priority register 3 (INT2PRI3)	H'FFD4 000C	H'001F 0000	DMAC (0) interrupt priority level: 31
Interrupt mask clear register (INT2MSKCR)	H'FFD4 003C	H'0000 0100	DMAC (0) interrupt mask clear
DMA source address register 0 (SAR0)	H'FC80 8020	H'E500E000	(Transfer source address)
DMA destination address register 0 (DAR0)	H'FC80 8024	H'08002000	(Transfer destination address)
DMA transfer count register 0 (TCR0)	H'FC80 8028	H' 1000	16 Kbytes ÷ 4 bytes = 4096
DMA channel control register 0 (CHCR0)	H'FC80 802C	H' 42005414	Repeat mode (SAR/DAR/TCR) Transfer in 4-byte (longword) units Transfer destination address is incremented. Transfer source address is incremented. Auto request mode Cycle-steal mode DMA ch0 interrupt requests are enabled.
DMA operation register 0 (DMAOR0)	H'FC80 8060	H'3001	Intermittent mode 64 DMA master enable



Note: * Since this program directly changes registers for peripheral functions, the MD bit (processing mode bit) is set to 1 (privileged mode).
If this bit is changed to "0" (user mode) and the function for setting operations is called, access to the registers for peripheral functions leads to an address error.

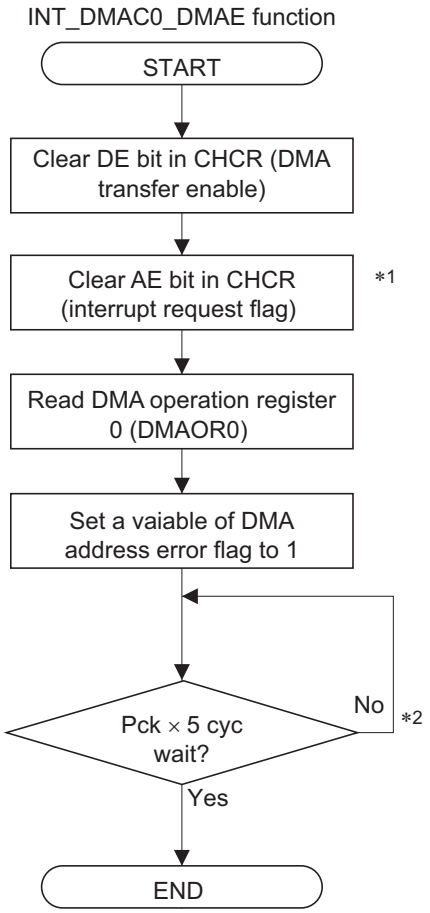
Figure 2 Flow of Processing by the Main Function of the Sample Program (Memory-to-Memory Transfer by the DMAC)



Notes: 1. When a DMA transfer-end interrupt is used, completion of the last transfer must be confirmed by a dummy-read from the destination space followed by issuing of a SYNCO instruction.

2. To prevent the erroneous acceptance of interrupts from sources that should have been updated, wait for the priority determination time (Pck × 5 cycles) after reading the on-chip module register that contains the given flag and before setting the BL bit to 0.

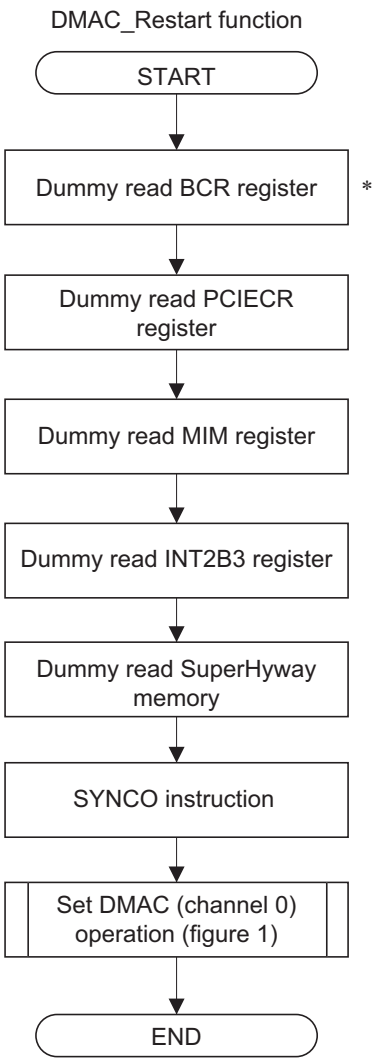
Figure 3 Flow of DMINT0 (DMA Transfer-End) Interrupt Handling



Notes: 1. To prevent the erroneous acceptance of interrupts from sources that should have been updated, wait for the priority determination time (Pck × 5 cycles) after reading the on-chip module register that contains the given flag and before setting the BL bit to 0.

2. When an address error occurs, its occurrence is recorded and a transition to the wait state is made.

Figure 4 Flow of Address Error Interrupt Handling



Note: * When a DMA address error occurs, the following steps should be performed before restarting transfer.

1. Dummy read to the following modules:
   - LBSC: BCR register
   - PCIC: PCIECR register
   - DDRIF: MIM register
   - INTC: LINT2B3 register
   - SuperHyway memory
2. Issue a SYNCO instruction.
3. Reconfigure all channels corresponding to the DMAOR where an address error occurred.

Figure 5 Flow of Processing to Restart DMA Transfer

3. Listing of Sample Program

1. Sample Program Listing: "dmac.c" (1)

```
/*""FILE COMMENT""*********************************************************************
*     System Name :   SH7780 Sample Program
*     File Name   :   dmac.c
*     Version     :   1.00.00
*     Contents    :   SH7780 DMAC transmit Program
*     Model       :   Hitachi_ULSI_Systems SolutionEngine MS7780SE03
*     CPU         :   SH7780
*     Compiler    :   SHC.9.1.00
*     OS          :   none
*
*     note        :   < Caution >
*                     This sample program is provided simply as a reference and
*                     its operation is not guaranteed.
*                     Use this sample program as a technical reference when
*                     developing software.
*
* Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
*
*     History     :   2007/12/26  ver 1.00.00
*
*******************************************************************************************/
#include <machine.h>

/* --- Function Definition(internal) --- */
void DMAC_Initialize(void);
void DMAC_Restart(void);

/* --- Symbol Definition --- */
struct st_dmac0{                                    /* struct DMAC0 */
             void           *SAR;                   /*      SAR     */
             void           *DAR;                   /*      DAR     */
             unsigned int   TCR;                    /*      TCR     */
             union{                                 /*      CHCR    */
                 unsigned int LONG;                 /* Long Word Access */
                 struct{                            /* Bit Access  */
                        unsigned int   :1;          /*              */
                        unsigned int LCKN :1;       /*      LCKN    */
                        unsigned int   :2;          /*              */
                        unsigned int RPT :3;        /*      RPT     */
                        unsigned int   :1;          /*              */
                        unsigned int DO :1;         /*      DO      */
                        unsigned int RL :1;         /*      RL      */
                        unsigned int   :1;          /*              */
                        unsigned int TS2 :1;        /*      TS2     */
                        unsigned int HE :1;         /*      HE      */
                        unsigned int HIE :1;        /*      HIE     */
                        unsigned int AM :1;         /*      AM      */
                        unsigned int AL :1;         /*      AL      */
                        unsigned int DM :2;         /*      DM      */
                        unsigned int SM :2;         /*      SM      */
                        unsigned int RS :4;         /*      RS      */
                        unsigned int DL :2;         /*      DL      */
                        unsigned int TB :1;         /*      TB      */
                        unsigned int TS :2;         /*      TS      */
```

2. Sample Program Listing: "dmac.c" (2)

```
                        unsigned int IE:1;        /*      IE      */
                        unsigned int TE:1;        /*      TE      */
                        unsigned int DE:1;        /*      DE      */
                    }   BIT;
                }   CHCR;
};

union st_dmac{                                    /* struct DMAOR */
                unsigned short WORD;              /* Word Access */
                struct{                           /* Bit Access  */
                    unsigned short     :2;        /*             */
                    unsigned short CMS :2;        /*      CMS    */
                    unsigned short     :2;        /*             */
                    unsigned short PR  :2;        /*      PR     */
                    unsigned short     :5;        /*             */
                    unsigned short AE  :1;        /*      AE     */
                    unsigned short NMIF:1;        /*      NMIF   */
                    unsigned short DME :1;        /*      BIT    */
                }   BIT;
};

#define DMAC0        (*(volatile struct st_dmac0   *)0xFC808020)  /* DMAC ch0 register top
                    Address */
#define DMAOR0       (*(volatile union st_dmac  *)0xFC808060)  /* DMAOR0 Address */

#define BCR          (*(volatile unsigned int   *)0xFF801000)
#define PCIECR       (*(volatile unsigned int   *)0xFE000008)
#define MIM_L        (*(volatile unsigned int   *)0xFE80000C)
#define INT2B3       (*(volatile unsigned int   *)0xFFD4004C)
#define SHMEM0_TOP_ADD   ((void *)0xFE410000)

#define INT2PRI3 (*(volatile unsigned int   *)0xFFD4000C)
#define INT2MSKCR    (*(volatile unsigned int   *)0xFFD4003C)  /* INT2MSKCR Address */

#define  LRAM_SRC_ADR       ((void  *)0xE500E000)  /* DMA source Address */
#define  DDR_DST_ADR        ((void  *)0x08002000)  /* DMA destination Address */

/***** Function Comment ****************************************
* Outline     : DMAC_Initialize
*-------------------------------------------------------------
* Declaration     : void DMAC_Initialize(void)
*-------------------------------------------------------------
* Functional description:
*               Initialize DMAC controller and start transmit
*-------------------------------------------------------------
* Return Value    : -
* Argument        : -
*-------------------------------------------------------------
* Input           : -
* Output      : -
*-------------------------------------------------------------
* Notes           : -
****** Function Comment End ***********************************/
void DMAC_Initialize(void)
{
  INT2PRI3 |= 0x001f0000;              /* DMAC ch0 interrupt level 31 */
```

3. Sample Program Listing: "dmac.c" (3)

```
  INT2MSKCR = 0x00000100;           /* DMAC ch0 interrupt mask clear */

  DMAC0.CHCR.BIT.DE = 0;            /* DMAC ch0 transmit disable */
  DMAC0.SAR = LRAM_SRC_ADR;         /* DMAC ch0 transmit source Address */
  DMAC0.DAR = DDR_DST_ADR;          /* DMAC ch0 transmit destination Address */
  DMAC0.TCR = 0x00001000;           /* DMAC ch0 transmit count */
  DMAC0.CHCR.LONG = 0x42005414;     /* DMAC ch0 CHCR set */
  DMAOR0.BIT.CMS = 0x03;            /* Intermittent mode 64 */
  DMAOR0.BIT.AE &= 0;               /* clear Address Error flag */
  DMAOR0.BIT.NMIF &= 0;             /* clear NMI interrupt flag */
  DMAOR0.BIT.DME = 1;               /* enable DMAC ch0 DMA master */
  DMAC0.CHCR.BIT.DE = 1;            /* enable DMAC ch0 transmite */
}

/***** Function Comment ***************************************
* Outline     : DMAC_ReStart
*------------------------------------------------------------
* Declaration    : void DMAC_Restart(void)
*------------------------------------------------------------
* Functional description:
*              restart DMA Controller transmit
*------------------------------------------------------------
* Return Value   : -
* Argument       : -
*------------------------------------------------------------
* Input          : -
* Output         : -
*------------------------------------------------------------
* Notes          : -
****** Function Comment End ***********************************/
void DMAC_Restart(void)
{
  volatile unsigned int dummy;

  dummy = BCR;                      /* dummy read BCR */
  dummy = PCIECR;                   /* dummy read PCIECR */
  dummy = MIM_L;                    /* dummy read MIM */
  dummy = INT2B3;                   /* dummy read INT2B3 */
  dummy = (*(unsigned int *)SHMEM0_TOP_ADD);    /* dummy read SuperHyway RAM */

  synco();                          /* SYNCO */

  DMAC_Initialize();
}
```

4. Sample Program Listing: "intprg.c" (1)

```
/*""FILE COMMENT""*********************************************************************
*     System Name :   SH7780 Sample Program
*     File Name   :   intprg.c
*     Version     :   1.00.00
*     Contents    :   SH7780 Initialize Program
*     Model       :   Hitachi_ULSI_Systems SolutionEngine MS7780SE03
*     CPU         :   SH7780
*     Compiler    :   SHC.9.1.00
*     OS          :   none
*
*     note        :   < Caution >
*                     This sample program is provided simply as a reference and
*                     its operation is not guaranteed.
*                     Use this sample program as a technical reference when
*                     developing software.
*
* Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
*
*     History     :   2007/12/26  ver 1.00.00
*
*******************************************************************************************/
#include <machine.h>

/* --- Function Definition(internal) --- */
static void int_responstime_wait(unsigned int wait_time);

/* --- Symbol Definition --- */
struct st_tmu{                                          /* struct TMU0  */
               unsigned int     TCOR;                   /*   TCOR       */
               unsigned int     TCNT;                   /    TCNT       */
               union {                                 /    TCR        */
                     unsigned short WORD;              /  Word Access */
                     struct {                          /  Bit  Access */
                            unsigned short     :7;      /              */
                            unsigned short UNF :1;      /    UNF       */
                            unsigned short     :2;      /              */
                            unsigned short UNIE:1;      /    UNIE      */
                            unsigned short CKEG:2;      /    CKEG      */
                            unsigned short TPSC:3;      /    TPSC      */
                            }       BIT;                /              */
                     }          TCR;                    /              */
};

union st_int2b3{
  unsigned int       LONG;          /* Long Word Access    */
  struct{                           /* Bit Access  */
      unsigned int           :18;   /*             */
      unsigned int   DMAE1   :1;    /*   DMAE1     */
      unsigned int   DMAE0   :1;    /*   DMAE0     */
      unsigned int   DMINT11 :1;    /*   DMINT11   */
      unsigned int   DMINT10 :1;    /*   DMINT10   */
      unsigned int   DMINT9  :1;    /*   DMINT9    */
      unsigned int   DMINT8  :1;    /*   DMINT8    */
      unsigned int   DMINT7  :1;    /*   DMINT7    */
      unsigned int   DMINT6  :1;    /*   DMINT6    */
      unsigned int   DMINT5  :1;    /*   DMINT5    */
```

5. Sample Program Listing: "intprg.c" (2)

```
      unsigned int   DMINT4  :1;     /*   DMINT4     */
      unsigned int   DMINT3  :1;     /*   DMINT3     */
      unsigned int   DMINT2  :1;     /*   DMINT2     */
      unsigned int   DMINT1  :1;     /*   DMINT1     */
      unsigned int   DMINT0  :1;     /*   DMINT0     */
  }BIT;
};

struct st_dmac0{                                     /* struct DMAC0 */
             void           *SAR;                    /*      SAR     */
             void           *DAR;                    /*      DAR     */
             unsigned int   TCR;                     /*      TCR     */
             union{                                  /*      CHCR    */
                 unsigned int LONG;                  /* Long Word Access */
                 struct{                             /* Bit Access  */
                         unsigned int   :1;          /*              */
                         unsigned int LCKN :1;       /*      LCKN    */
                         unsigned int   :2;          /*              */
                         unsigned int RPT :3;        /*      RPT     */
                         unsigned int   :1;          /*              */
                         unsigned int DO :1;         /*      DO      */
                         unsigned int RL :1;         /*      RL      */
                         unsigned int   :1;          /*              */
                         unsigned int TS2 :1;        /*      TS2     */
                         unsigned int HE :1;         /*      HE      */
                         unsigned int HIE :1;        /*      HIE     */
                         unsigned int AM :1;         /*      AM      */
                         unsigned int AL :1;         /*      AL      */
                         unsigned int DM :2;         /*      DM      */
                         unsigned int SM :2;         /*      SM      */
                         unsigned int RS :4;         /*      RS      */
                         unsigned int DL :2;         /*      DL      */
                         unsigned int TB :1;         /*      TB      */
                         unsigned int TS :2;         /*      TS      */
                         unsigned int IE:1;          /*      IE      */
                         unsigned int TE:1;          /*      TE      */
                         unsigned int DE:1;          /*      DE      */
                 }   BIT;
             }   CHCR;
};

union st_dmac{                                       /* struct DMAOR */
             unsigned short WORD;                    /* Word Access */
             struct{                                 /* Bit Access  */
                 unsigned short     :2;              /*              */
                 unsigned short CMS :2;              /*      CMS     */
                 unsigned short     :2;              /*              */
                 unsigned short PR  :2;              /*      PR      */
                 unsigned short     :5;              /*              */
                 unsigned short AE  :1;              /*      AE      */
                 unsigned short NMIF:1;              /*      NMIF    */
                 unsigned short DME :1;              /*      BIT     */
             }   BIT;
};

```

6. Sample Program Listing: "intprg.c" (3)

```
#define DMAC0        (*(volatile struct st_dmac0   *)0xFC808020)  /* DMAC ch0 register top
                    Address */
#define DMAOR0       (*(volatile union st_dmac  *)0xFC808060)  /* DMAOR0 Address */

#define INT2B3   (*(volatile union st_int2b3 *)0xFFD4004C) /* INT2B3 Address */

#define TMU0 (*(volatile struct st_tmu  *)0xFFD80008)  /* TMU0  Address */
#define  DDR_TOP_ADR    (*(volatile unsigned int *)0x08000000)

#define INTC_RESPONSEWAIT   (0x00000014)       /* INT response wait Pck 5cycle
                                              H'14 = (1/Pck*5cyc) / (1/Ick*3cyc) */

/* --- RAM allocation variable declaration --- */
extern unsigned char u1Flg5ms;
extern unsigned char u1FlgEndDmac0;
extern unsigned char u1FlgAddErrDMAC0;
#pragma section IntPRG

/* H'580 TMU ch-0 underflow interrupt */
void INT_TMU0_TUNI0(void)
{
  volatile unsigned short dummy;

  TMU0.TCR.BIT.UNF = 0;      /* TMU ch0 UNF flag clear */
  u1Flg5ms = 1;              /* set 5ms flag */
  dummy = TMU0.TCR.WORD; /* dummy read */

  int_responstime_wait(INTC_RESPONSEWAIT);  /* 5cyc(Pck=33MHz) wait */
}

/* H'640 ch-0 DMA transmit end or halfend interrupt */
void INT_DMAC0_DMINT0(void)
{                               /* (start of additional part from Initialize program) */
  volatile unsigned int dummy;

  dummy = DDR_TOP_ADR;              /* destinate address dummy read */
  synco();                          /* SYNCO */

  u1FlgEndDmac0 = 1;                /* set"DMAC ch0 transmit end flag" */

  DMAC0.CHCR.BIT.DE = 0;            /* DMAC ch0 transmite disable */
  DMAC0.CHCR.BIT.TE &= 0;           /* DMAC ch0 TEbit clear */

  dummy = DMAC0.CHCR.LONG;          /* dummy read */

  int_responstime_wait(INTC_RESPONSEWAIT);  /* 5cyc(Pck=33MHz) wait */
}                               /* (end of additional part from Initialize program) */
/* H'660 ch-1 DMA transmit end or halfend interrupt */
void INT_DMAC0_DMINT1(void)
{
}
/* H'680 ch-2 DMA transmit end or halfend interrupt */
void INT_DMAC0_DMINT2(void)
{
}
```

7. Sample Program Listing: "intprg.c" (4)

```
/* H'6A0 ch-3 DMA transmit end or halfend interrupt */
void INT_DMAC0_DMINT3(void)
{
}
/* H'6C0 ch0-5,ch6-11 DMA address error interrupt */
void INT_DMAC0_DMAE(void)
{                               /* (start of additional part from Initialize program) */
  volatile unsigned int dummy;

  DMAC0.CHCR.BIT.DE = 0;        /* DMAC ch0 transmit disable */
  DMAOR0.BIT.AE &= 0;           /* clear address error flag */

  dummy = DMAOR0.WORD;          /* dummy read */

  u1FlgAddErrDMAC0 = 1;         /* set "DMAC ch0-5 address error flag" */

  int_responstime_wait(INTC_RESPONSEWAIT);  /* 5cyc(Pck=33MHz) wait */
}                               /* (end of additional part from Initialize program) */

#pragma inline_asm(int_responstime_wait)
static void int_responstime_wait(unsigned int wait_time)
{
?0001:
            DT          R4
            BF          ?0001
            NOP
}
```

8. Sample Program Listing: "main.c" (1)

```
/*""FILE COMMENT""*********************************************************************
*     System Name :   SH7780 Sample Program
*     File Name   :   main.c
*     Version     :   1.00.00
*     Contents    :   SH7780 Initialize Program
*     Model       :   Hitachi_ULSI_Systems SolutionEngine MS7780SE03
*     CPU         :   SH7780
*     Compiler    :   SHC.9.1.00
*     OS          :   none
*
*     note        :   < Caution >
*                     This sample program is provided simply as a reference and
*                     its operation is not guaranteed.
*                     Use this sample program as a technical reference when
*                     developing software.
*
* Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
*
*     History     :   2007/12/26  ver 1.00.00
*
*******************************************************************************************/
#include <machine.h>

/* --- Function Definition(internal) --- */

/* --- Symbol Definition --- */
struct st_dmac0{                                    /* struct DMAC0 */
             void           *SAR;                   /*      SAR     */
             void           *DAR;                   /*      DAR     */
             unsigned int   TCR;                    /*      TCR     */
             union{                                 /*      CHCR    */
                 unsigned int LONG;                 /* Long Word Access */
                 struct{                            /* Bit Access  */
                         unsigned int   :1;         /*              */
                         unsigned int LCKN :1;      /*      LCKN    */
                         unsigned int   :2;         /*              */
                         unsigned int RPT :3;       /*      RPT     */
                         unsigned int   :1;         /*              */
                         unsigned int DO :1;        /*      DO      */
                         unsigned int RL :1;        /*      RL      */
                         unsigned int   :1;         /*              */
                         unsigned int TS2 :1;       /*      TS2     */
                         unsigned int HE :1;        /*      HE      */
                         unsigned int HIE :1;       /*      HIE     */
                         unsigned int AM :1;        /*      AM      */
                         unsigned int AL :1;        /*      AL      */
                         unsigned int DM :2;        /*      DM      */
                         unsigned int SM :2;        /*      SM      */
                         unsigned int RS :4;        /*      RS      */
                         unsigned int DL :2;        /*      DL      */
                         unsigned int TB :1;        /*      TB      */
                         unsigned int TS :2;        /*      TS      */
                         unsigned int IE:1;         /*      IE      */
                         unsigned int TE:1;         /*      TE      */
                         unsigned int DE:1;         /*      DE      */
                 }   BIT;
```

9. Sample Program Listing: "main.c" (2)

```
            }   CHCR;
};

union st_dmac{                                      /* struct DMAOR */
            unsigned short WORD;                    /* Word Access */
            struct{                                 /* Bit Access  */
                unsigned short     :2;              /*             */
                unsigned short CMS :2;              /*     CMS     */
                unsigned short     :2;              /*             */
                unsigned short PR  :2;              /*     PR      */
                unsigned short     :5;              /*             */
                unsigned short AE  :1;              /*     AE      */
                unsigned short NMIF:1;              /*     NMIF    */
                unsigned short DME :1;              /*     BIT     */
            }   BIT;
};

#define DMAC0        (*(volatile struct st_dmac0   *)0xFC808020)  /* DMAC ch0 register top
                Address */

#define  SR_Init        0x400000e0         /* Privileged mode, IMASK level 14 */

/* --- RAM allocation variable declaration --- */
volatile unsigned char u1Flg5ms;
volatile unsigned char u1Cnt1s;
volatile unsigned char u1FlgEndDmac0;
volatile unsigned char u1FlgAddErrDMAC0;

/***** Function Comment ****************************************
* Outline    : main
*-------------------------------------------------------------
* Declaration    : void main(void)
*-------------------------------------------------------------
* Functional description:
*              main function
*-------------------------------------------------------------
* Return Value   : -
* Argument       : -
*-------------------------------------------------------------
* Input          : -
* Output     : -
*-------------------------------------------------------------
* Notes          : -
****** Function Comment End ***********************************/
void main(void)
{
  set_cr(SR_Init);          /* Set SR "Privileged mode, IMASK level 14" */

  TMU0_Initialize();        /* TMU0 Initialize (additional part from Initialize program)*/
  DMAC_Initialize();        /* DMAC Initialize (additional part from Initialize program)*/

  while(1)
  {                         /* (start of additional part from Initialize program) */
      while(u1Flg5ms == 0x00)
      {
          nop();
```

10. Sample Program Listing: "main.c" (3)

```
    }
    u1Flg5ms = 0;              /* clear 5ms flag */
    u1Cnt1s++;                 /* 1s count +1 */

    if(u1FlgEndDmac0 == 1)     /* if DMAC-ch0 transmit end */
    {
        DMAC0.CHCR.BIT.DE = 1; /* DMAC ch0 transmit enable */
        u1FlgEndDmac0 = 0;     /* clear "DMAC ch0 transmit end flag" */
    }
    if(u1FlgAddErrDMAC0 == 1)
    {
        DMAC_Restart();        /* DMAC-ch0 transmit restart */
        u1FlgAddErrDMAC0 = 0;
    }
  }                            /* (end of additional part from Initialize program) */
}
```

11. Sample Program Listing: "vecttbl.src"

```
;*""FILE COMMENT""*********************************************************************
;     System Name :   SH7780 Sample Program
;     File Name   :   vecttbl.src
;     Version     :   1.00.00
;     Contents    :   SH7780 Initialize Program
;     Model       :   Hitachi_ULSI_Systems SolutionEngine MS7780SE03
;     CPU         :   SH7780
;     Compiler    :   SHC.9.1.00
;     OS          :   none
;
;     note        :   < Caution >
;                     This sample program is provided simply as a reference and
;                     its operation is not guaranteed.
;                     Use this sample program as a technical reference when
;                     developing software.
;
; Copyright (C) 2007 Renesas Technology Corp. All Rights Reserved
;
;     History     :   2007/12/26  ver 1.00.00
;
;*******************************************************************************************/

              .include    "vect.inc"

              .section    VECTTBL,data
              .export     _RESET_VECTORS

;TMU-ch0
              ;H'580      TMU_TUNI0
              .data.b      H'F0

;DMAC(0)
              ;H'640      DMINT0
               .data.b     H'F0        /* (change part from Initialize program) */
              ;H'660      DMINT1
               .data.b     H'00
              ;H'680      DMINT2
               .data.b     H'00
              ;H'6A0      DMINT3
               .data.b     H'00
              ;H'6C0      DMAE
               .data.b     H'F0        /* (change part from Initialize program) */
              ;H'6E0      reserve
               .data.b     H'00
```

4. Documents for Reference

- Hardware Manual
  SH7780 Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Software Manual
  SH-4A Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

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Revision Record

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