Solder Reflow Guide for Surface Mount Devices

April 2008 Technical Note TN1076

Introduction

This technical note provides general guidelines for a solder reflow and rework process for Lattice surface mount products. The data used in this document is based on IPC/JEDEC standards. Each board has its own profile which depends upon the reflow equipment used and the board design. The PCB must be individually characterized to find the reliable profile. This document covers both the SnPb Eutectic process and the Pb-Free process.

Reflow

- Use caution when profiling to insure the maximum temperature difference between components is less than 10°C (7°C within an individual component).
- Forced convection reflow with nitrogen is preferred (with maximum oxygen content of 50-75 PPM).

Inspection

- Pre-reflow: Use visual inspection to verify solder paste dispense location and quantity.
- Pick and Place: Use machine vision as necessary to ensure proper component placement.
- Post reflow: Use electrical testing to verify solder joint formation (100% post-reflow visual inspection is not recommended).

Cleaning Recommendations

- After solder reflow, printed circuit boards should be thoroughly cleaned and dried using standard cleaning equipment.
- Final rinse should be warm DI water (50° to 75°C) with resistivity of 0.2 Meg Ohms/cm or greater.
- After cleaning, boards should be baked for a minimum of 1 hour at 125°C to evaporate residual moisture.

Rework Recommendations

Removal and replacement of SMT packages on printed circuit boards is fairly straightforward. However, reattachment or touch-up of SMT packages that have already been soldered to the board is not practical in most cases.

A few important criteria should be considered when choosing a rework system:

- Minimize the change in temperature across the solder joint array to promote good solder joint formation, minimize intermetallic growth, improve solderability and minimize component warpage.
- Minimize die temperature to prevent die delamination and wire bond failure.
- Minimize board temperature adjacent to the rework site to reduce intermetallic growth, prevent secondary reflow, and prevent possible component delamination.
- For boards with no internal ground plane, apply localized heat to the SMT package. When the solder is molten, remove package using appropriate vacuum tool.
- While the board is still hot, remove excess solder from the site using a vacuum desoldering system or a soldering iron and solder wicking material. Use care to avoid damaging the solder pads or the surrounding solder mask.
- For PCBs with internal ground plane(s), preheat the entire board to at least 80°C before removing the SMT packages.

© 2008 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- Use alcohol to remove residual flux, then wash the entire board using the standard board cleaning process before attempting to replace SMT components.

BGA Reballing

BGA reballing is not recommended. Reballed BGA packages will void the original Lattice specifications.

Pb-Free/RoHS-Compliant Products

All Lattice Pb-Free products are also fully RoHS compliant. Lattice offers a broad range of Pb-Free/RoHS-compliant products in a variety of package configurations. These packages include the Thin Quad Flat Pack (TQFP), Quad Flat Pack (QFN), Fine Pitch BGA (fpBGA), Fine Pitch Super BGA (fpSBGA) and Chip-Scale BGA (csBGA).

Peak Reflow Temperature (T_P) by Package Size

Table 1 illustrates the peak reflow temperatures by package size. Refer to the *Package Diagrams* document on the Lattice web site at www.latticesemi.com. Use maximum package dimensions to determine package thickness and volume.

Table 1. Peak Reflow Temperature (T_P)

Classification	Package Thickness	Volume < 350 mm^3	Volume = 350 - 2000 mm^3	Volume > 2000 mm^3
SnPb Eutectic Package	< 2.5 mm	240 + 0/-5°C	225 + 0/-5°C	
	≥ 2.5 mm	225 + 0/-5°C		
Pb-Free Package	< 1.6 mm	260 + 0/-5°C		
	1.6 mm to < 2.5 mm	260 + 0/-5°C	250 + 0/-5°C	245 + 0/-5°C
	≥ 2.5 mm	250 + 0/-5°C	245 + 0/-5°C	

Note: Package volume excludes external terminals (balls, bumps, lands, leads) and non-integral heat sinks.

Tables 2 and 3 show the peak reflow temperature for Lattice devices by package type and size.

Table 2. Peak Reflow Temperature (T_P) by Package Type and Size, SnPb Packages

Package Type	Number of Leads/Balls	Moisture Sensitivity Level	Peak Reflow Temp (+0/-5°C)
caBGA	49	3	240
	100	3	240
	100	3	240
csBGA	56	3	240
	64	3	240
	100	3	240
	132	3	240
	144	3	240
fcBGA	1020	4	225
	1152	4	225
	1704	4	225

Table 2. Peak Reflow Temperature (T_P) by Package Type and Size, SnPb Packages (Continued)

Package Type	Number of Leads/Balls	Moisture Sensitivity Level	Peak Reflow Temp (+0/-5°C)
fpBGA	100	3	240
	144	3	240
	208	3	225
	256	3	225
	388	3	225
	416	3	225
	484	3	225
	516	3	225
	672	3	225
	676	3	225
	680	3	225
	900	3	225
	1152	3	225
	1156	3	225
fpBGA with Heat Sink	516	3	225
	680	3	225
fpSBGA	680	3	225
	1036	4	225
ftBGA	256	3	225
	324	3	225
TQFP (thickness: 1.4mm)	48	3	240
	64	3	240
	100	3	240
	128	3	240
	144	3	225
	176	3	225
TQFP (thickness: 1.0mm)	44	3	240
	48	3	240
BGA	272	3	225
	388	3	225
	492	3	225
PLCC	20	1	225
	28	1	225
	44	3	225
	68	3	225
	84	3	225
PQFP	100	3	225
	120	3	225
	128	3	225
	144	3	225
	160	3	225
	208	3	225
	240	3	225
	304	3	225

Table 2. Peak Reflow Temperature (T_P) by Package Type and Size, SnPb Packages (Continued)

Package Type	Number of Leads/Balls	Moisture Sensitivity Level	Peak Reflow Temp (+0/-5°C)
PQFP with External Heat Sink	208	3	225
	240	3	225
	304	3	225
PQFP with Heat Sink	160	3	225
	208	3	225
QFN	32	1	240
SBGA	256	3	225
	320	3	225
	352	3	225
	432	3	225
	600	3	225
SOIC	16	1	225
	20	1	225
	24	1	225
	28	1	225
SSOP	28	1	225

Table 3. Peak Reflow Temperature (T_P) by Package Type and Size, Pb-Free Packages

Package Type	Number of Leads/Balls	Moisture Sensitivity Level	Peak Reflow Temp (+0/-5°C)
caBGA	49	3	260
	100	3	260
csBGA	56	3	260
	64	3	260
	100	3	260
	132	3	260
	144	3	260
fcBGA	1020	4	245
	1152	4	245
	1704	4	245
fpBGA	100	3	260
	144	3	250
	208	3	250
	256	3	250
	388	3	250
	484	3	250
	516	3	250
	672	3	250
	680	3	250
	900	3	250
	1152	3	250
	1156	3	250
ftBGA	256	3	260
	324	3	260

Table 3. Peak Reflow Temperature (T_P) by Package Type and Size, Pb-Free Packages (Continued)

Package Type	Number of Leads/Balls	Moisture Sensitivity Level	Peak Reflow Temp (+0/-5°C)
TQFP (thickness: 1.4mm)	44	3	260
	48	3	260
	64	3	260
	100	3	260
	128	3	260
	144	3	260
	176	3	260
TQFP (thickness: 1.0mm)	44	3	260
	48	3	260
BGA	272	3	250
	388	3	250
PLCC	20	1	250
	28	1	245
	44	3	245
	84	4	245
PQFP	100	3	245
	120	3	245
	128	3	245
	144	3	245
	160	3	245
	208	3	245
QFN	32	1	260
SBGA	256	4	250
	320	4	250
	352	4	250
	432	4	245
	680	4	245

Reflow Profile for SMT Packages

The typical reflow process includes four phases.

1. **Preheat** – Brings the assembly from 25°C to T_S. During this phase the solvent evaporates from the solder paste. Preheat temperature ramp rate should be less than 2°C/second to avoid solder ball spattering and bridging.

   - Solder Ball Spattering – The most common solder balling defect is spattering which is caused by explosive evaporation of solvents. It can be eliminated by a slower temperature rise in the preheat phase.
   - Bridging – Often seen on fine pitch components and usually caused by inaccurate or splashy screen printing. But it can also be a result of solder paste slumping caused by rapid temperature rise in the preheat phase.

2. **Flux Activation** – The temperature rises slowly and reaches a point at which the flux completely wets the surfaces to be soldered.

3. **Reflow** – In this phase, the temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.

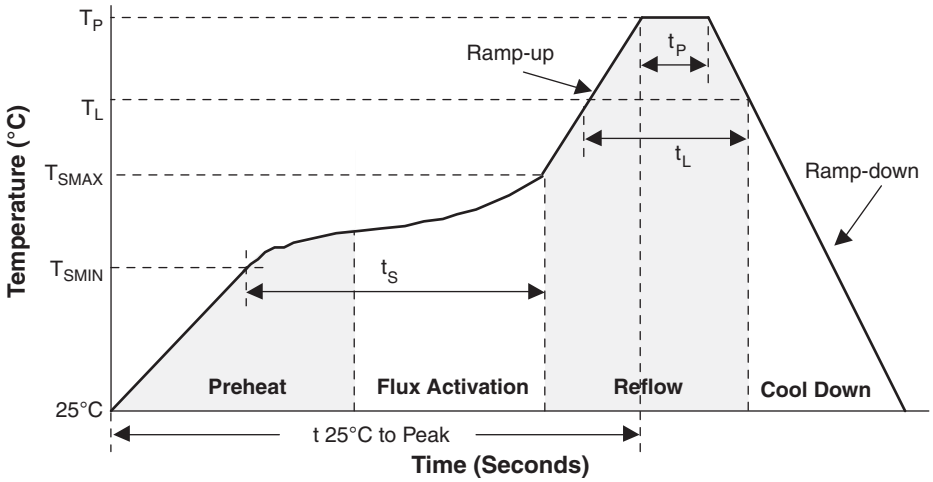
4. **Cool Down** – Ramp down rate should be as fast as possible in order to control grain size, but should not exceed 6°C/second.

Table 4 and Figure 1 describe the reflow profile.

Table 4. Reflow Profiles

Parameter	Description	Sn-Pb Eutectic Package	Pb-Free Package
Ramp-Up	Average Ramp-Up Rate (T_{SMAX} to T_P)	3°C/second max.	3°C/second max.
T_{SMIN}	Preheat Peak Min. Temperature	100°C	150°C
T_{SMAX}	Preheat Peak Max. Temperature	150°C	200°C
t_S	Time between T_{SMIN} and T_{SMAX}	60-120 seconds	60-180 seconds
T_L	Solder Melting Point	183°C	217°C
t_L	Time Maintained above T_L	60-150 seconds	60-150 seconds
t_P	Time within 5°C of Peak Temperature	10-30 seconds	20-40 seconds
Ramp-Down	Ramp-Down Rate	6°C/second max.	6°C/second max.
t 25°C to T_P	Time from 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Figure 1. Thermal Reflow Profile



Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
April 2008	02.2	Updated Peak Reflow Temperature (TP) by Package Type and Size table.