PSoC® 3 Magnetic Card Reader

AN54374

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Associated Application Notes: None

Application Note Abstract

This application note describes the PSoC® 3 implementation of a four-track magnetic card reader (MCR) with the automatic gain control (AGC) feature. Another feature of this design is the detection of bits at the peaks, which gives higher accuracy. The AGC compensates the amplitude variations. This design uses the differentiator method to detect the bits at the peaks, as compared to normal zero crossing detectors.

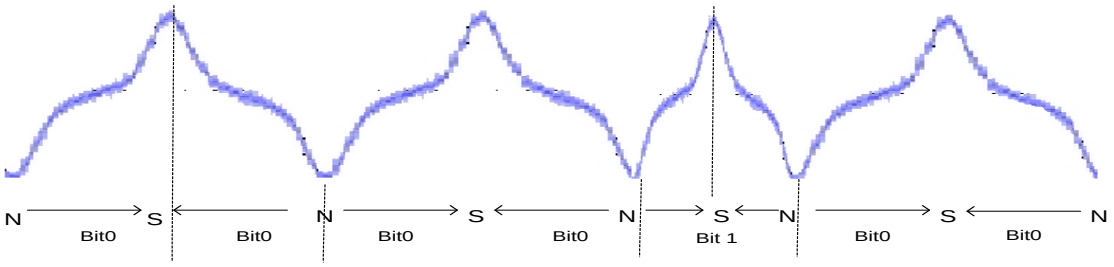
Introduction

This application note describes a four-track magnetic card reader and its implementation in PSoC 3 using the AGC feature. Magnetic cards have magnetic material, either embedded or on the exterior of the card. The magnetic head gives out a characteristic waveform when a card is swiped. When the card is swiped, the flux linked to the magnetic read head changes and produces a voltage. The magnetic stripe polarity and the voltage pulses generated from it are shown in Figure 1.

As shown in this figure, bit 0 makes two transitions at the edges. Bit 1 makes one more transition at the center in addition to the edges. This type of coding of data is called F2F, because if bit 0 gives frequency F, then bit 1 gives frequency 2F.

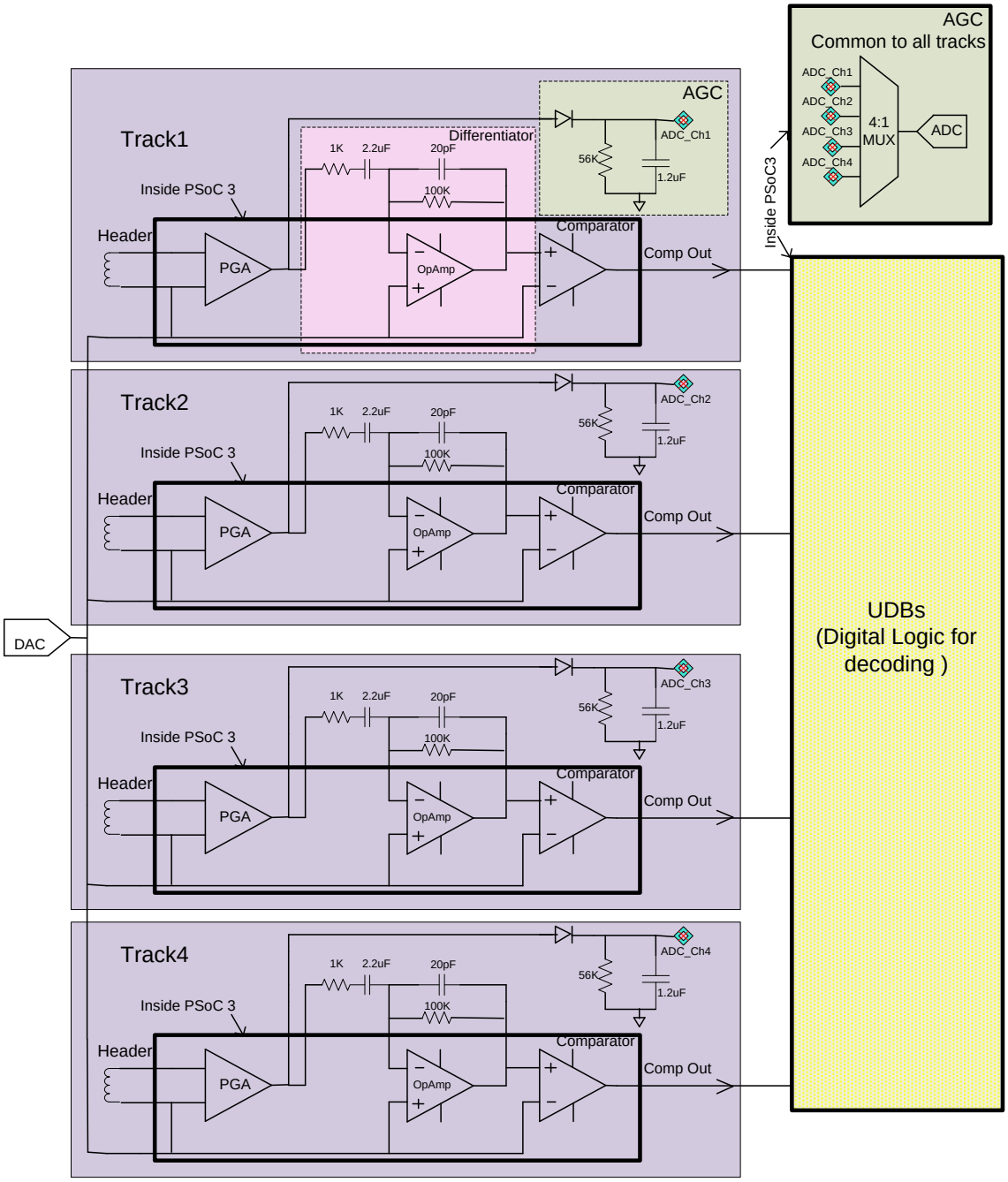
PSoC 3 can detect these pulses and decode the data. The method used in this design is the differentiator method that detects pulses at the peaks. PSoC 3 has enough resources to implement the design comprehensively: four PGAs, four opamps, four comparators, and a delta sigma ADC.

Figure 1. Magnetic Card Waveform



Working of the Design

Figure 2. Block Diagram



All the tracks of the magnetic head are biased at a reference DC voltage. The output of each track of the magnetic head is given to the PGA. The PGA provides the required gain for the header output, because it is very small (in the range of few mV to tens of mV).

The amplitude level of the magnetic head varies through the card swipe. The reasons for this could be the defects on the magnetic card or the variation in the speed of the swipe. A faster swipe produces larger flux change on the magnetic head, resulting in higher amplitude of voltage. Similarly, a slower swipe produces lesser flux change on the magnetic head, resulting in a lesser amplitude of voltage. This reference design has the AGC feature to compensate for these amplitude variations, so it maintains the accuracy of the detection amid voltage level variations. Automatic gain adjustment is done in the PGA by varying the gain of the PGA to adjust the amplitude level. The AGC is explained in detail in the section AGC on page 5.

The design scans for the occurrence of peaks in the waveform. Most ASICs follow a similar technique to convert the waveform to digital. The strategy is to get a digital output that has transitions corresponding to each peak of the waveform. This is achieved by using a differentiator that gives zero crossing at the peaks (see the waveforms in Figure 5 on page 4). The differentiator output goes into the comparator to produce the digital output.

The differentiator is implemented with the opamp in PSoC 3 and external components. The magnetic cards have a bit density of around 75 to 210 bits per inch. The swipe speeds typically vary from 5 inches per second to 50 inches per second. This produces waveforms in the frequency range of 375 Hz to 21 kHz.

The differentiator circuit is shown in Figure 3 and the gain and phase response are shown in Figure 4. The differentiator must be designed to have a 90 degree phase throughout the frequency range of operation. The gain of the differentiator increases linearly with frequency.

Since we are concerned about the zero crossings of the differentiator output here, the differentiator gain variation does not cause a problem. However, the designer must ensure that the differentiator output is not saturated or below the comparator hysteresis throughout the frequency range. The values R1, R2, C1, and C2 are tuned to get the desired frequency response.

Figure 3. Differentiator

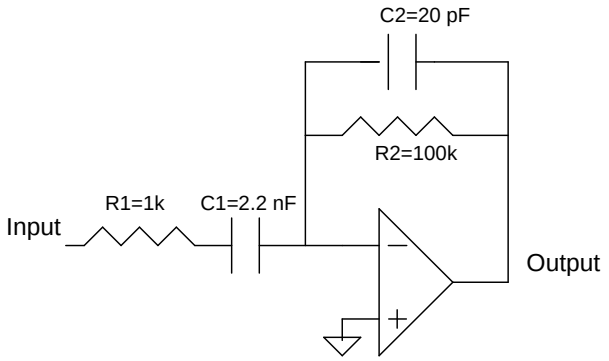
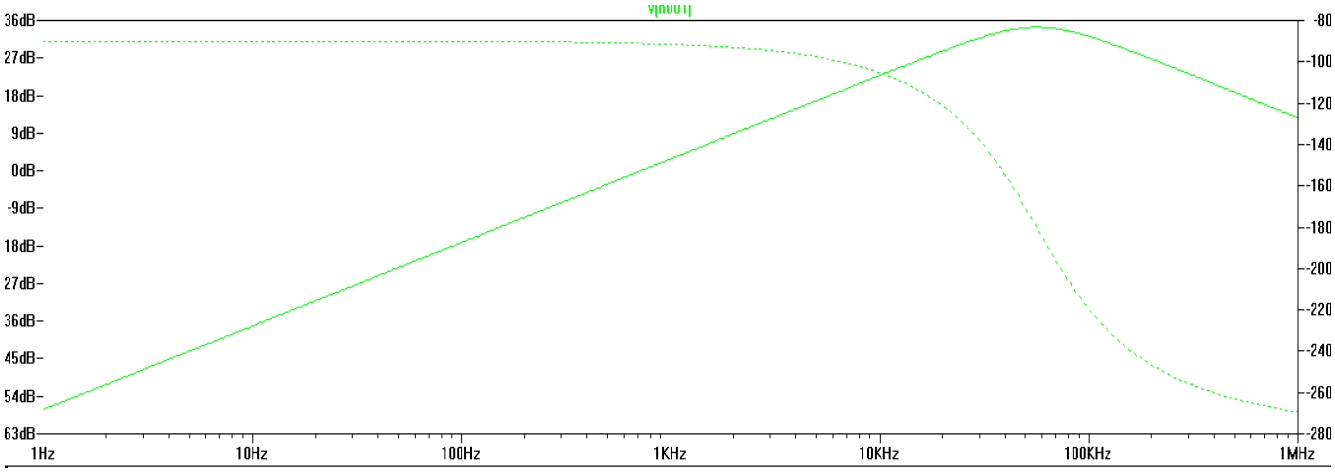


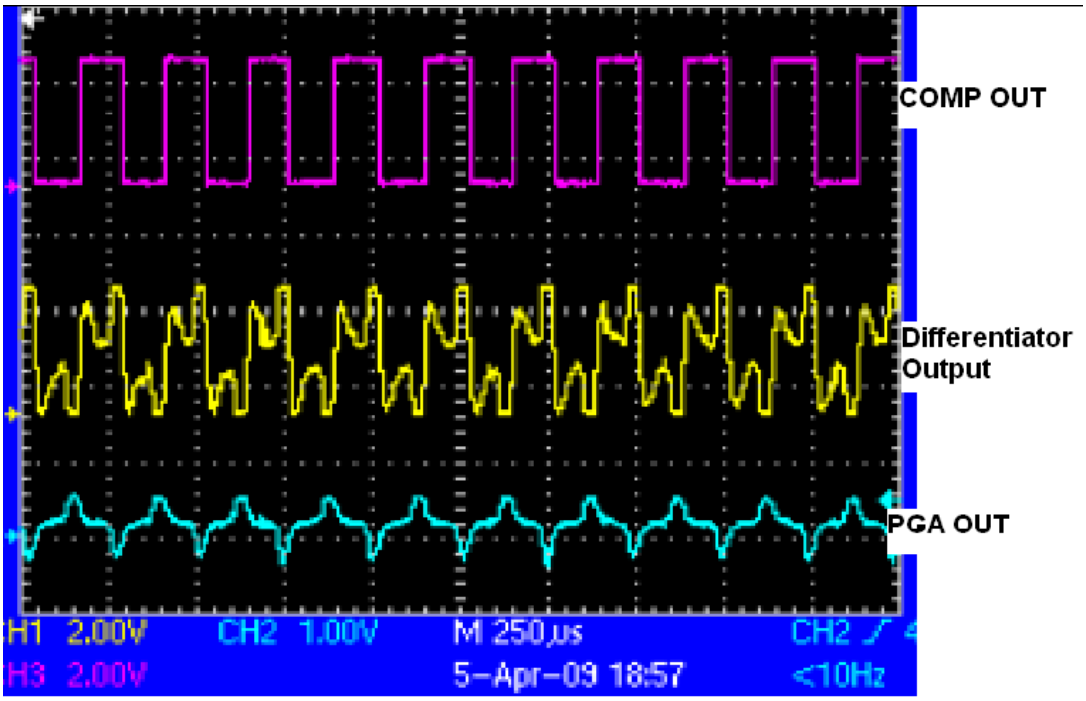
Figure 4. Differentiator Frequency Response



The comparator is configured to have a hysteresis and outputs a digital waveform transitioning at the peaks of the input wave. The waveforms shown in Figure 5 on page 4 illustrate the differentiator and comparator outputs. The digital waveform received from the comparator is the pulse width modulated wave representing 0s and 1s. This comparator output is passed to the Universal Digital Block (UDB) for further processing. The glue logic built in the UDB decodes the data on the card.

Note This project explains only the analog interface of the magnetic card reader; the end output of the project is the comparator output. Users can add their firmware and digital logic to the project for complete decoding of the information on the card. In the design provided, the AGC is shown on only one track. For other tracks, the channels are multiplexed onto the ADC.

Figure 5. Differentiator and Comparator Output



AGC

AGC uses an external peak detector in each channel to detect the amplitude level of the signal. The peak detector output is read by the ADC; a single ADC is used to read all the tracks. This is achieved by multiplexing each peak detector output to the ADC (see Figure 1 on page 1). Because the data required is not high precision, an 8-bit resolution for this measurement is sufficient. The 8-bit resolution provides enough speed (375 Ksps) to multiplex 4-channel data using the ADC. While multiplexing, each channel must lose the first three samples after the channel switch. As a result, the speed of ADC is effectively 375/4 = 94 Ksps. Because four channels are being multiplexed, the speed available for each channel is 94/4 = 23 Ksps. Since the waveform that the ADC is measuring is an inherently slower waveform of a peak detector, this speed is good enough for an effective AGC. Upon each conversion in ISR the ADC value is compared with the predetermined threshold levels and the PGA gain is adjusted to keep the amplitude between the two thresholds. The AGC algorithm is explained in Figure 6.

Note that in the design provided, the AGC is shown on only one track. For other tracks, the channels are multiplexed to the ADC.

Figure 6. AGC Algorithm

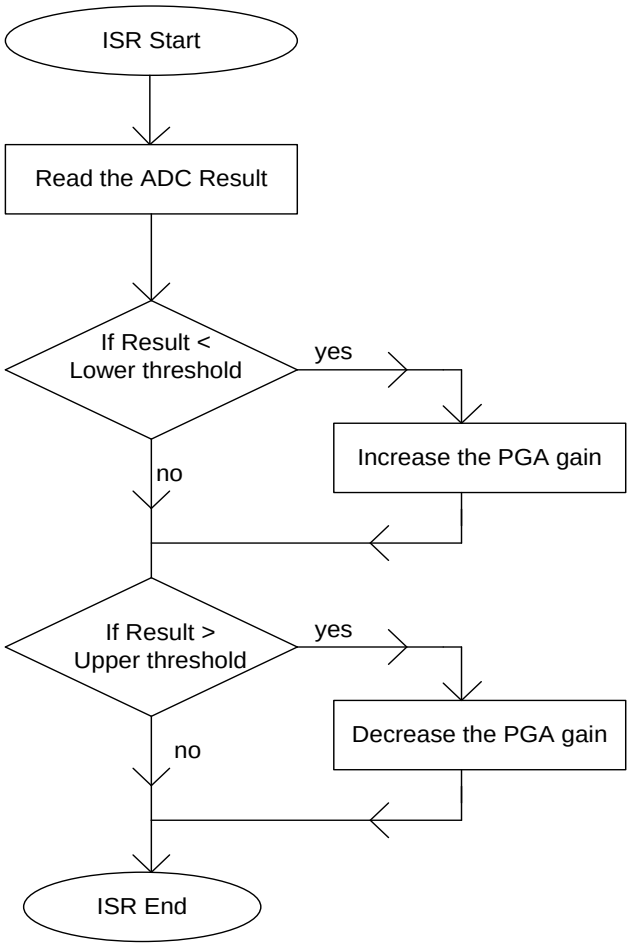
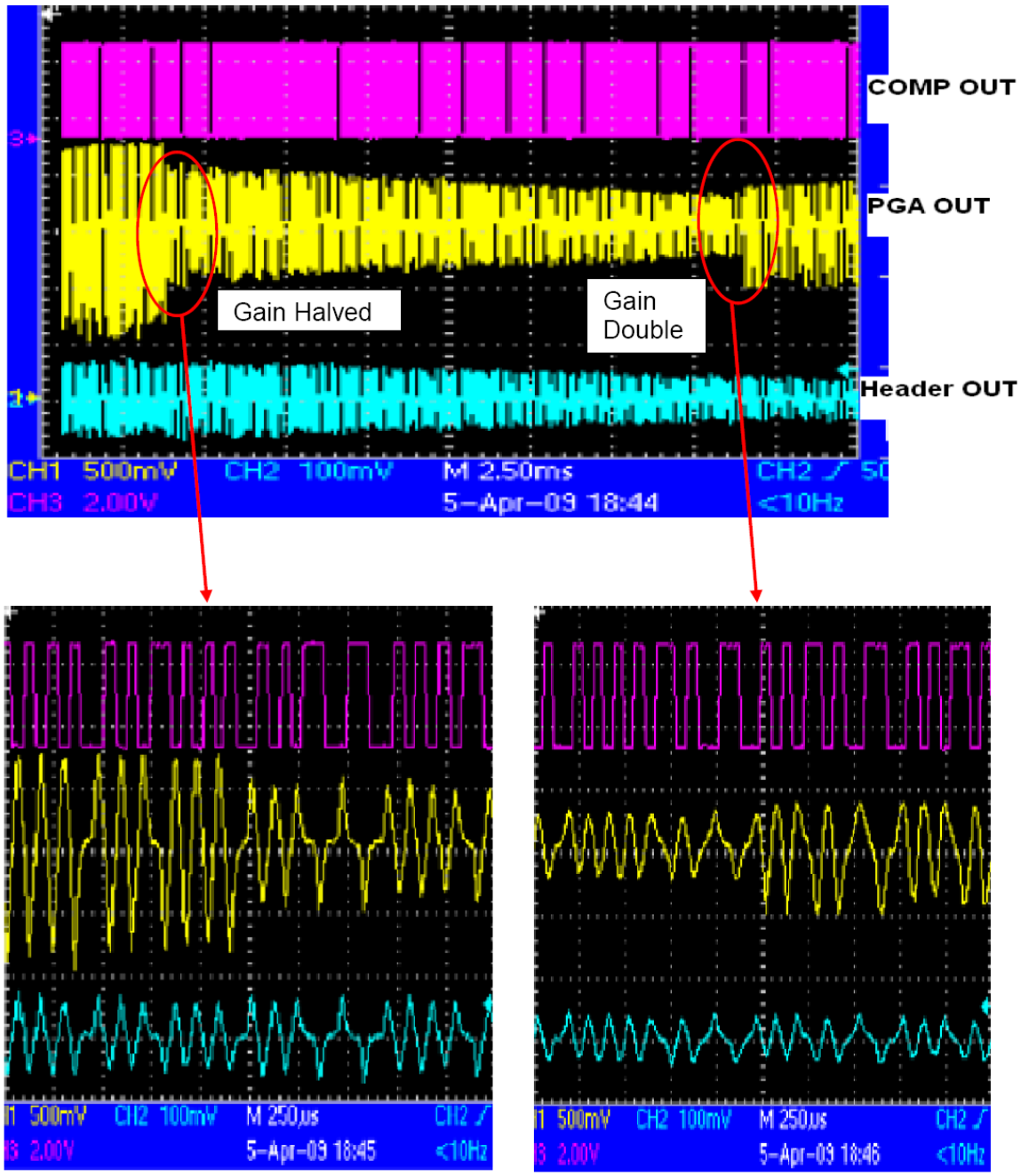


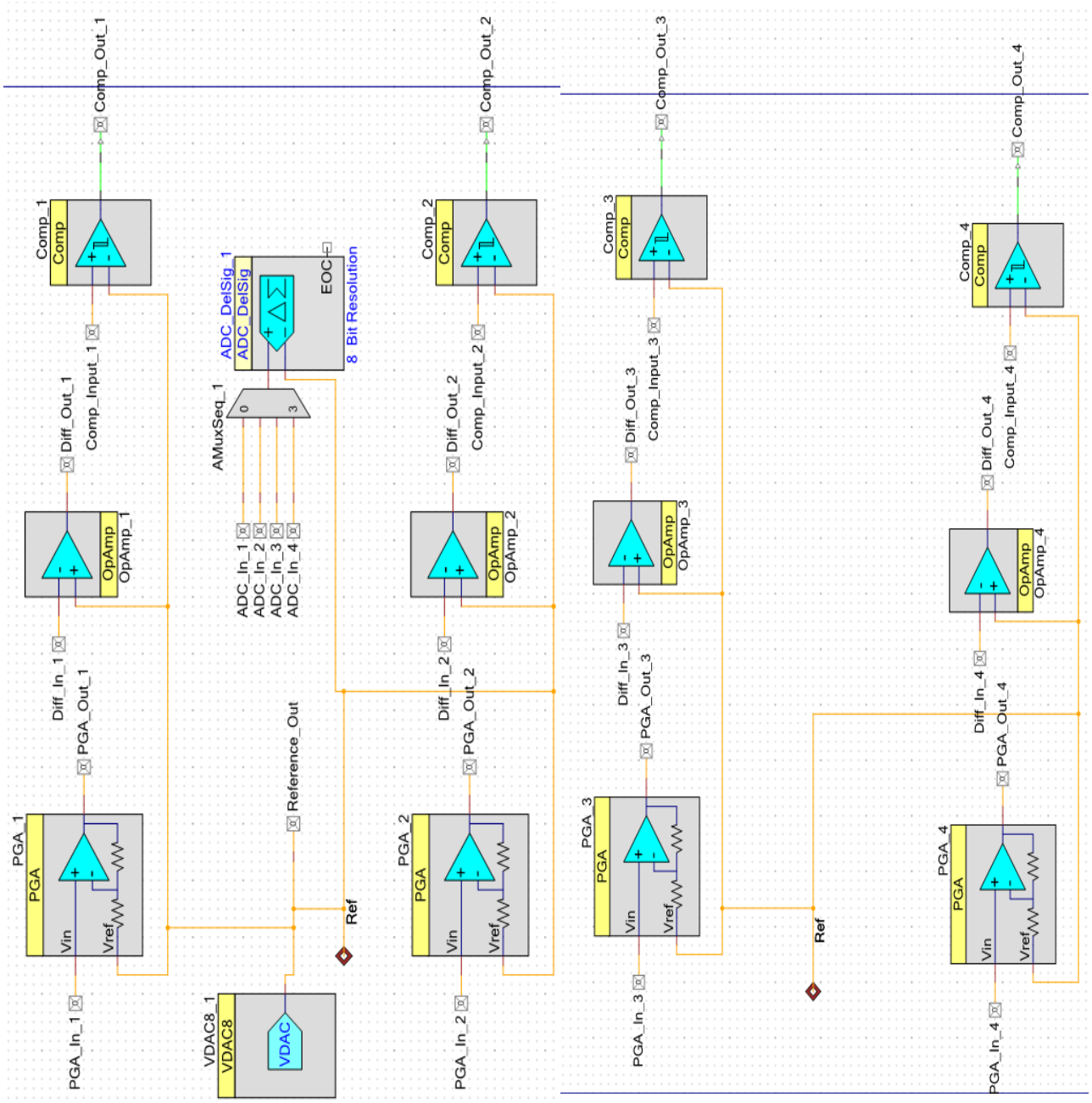
Figure 7. AGC Waveforms



PSoC 3 Implementation

Figure 8 shows the Top Design of the project. AGC is implemented in firmware, so the code mainly has AGC apart from the start APIs for all the blocks.

Figure 8. Top Design



The VDAC here is designed to provide a reference voltage to the magnetic card reader head. This can also be achieved by a reference voltage on an SIO pin with regulated output.

Table 1 lists the resource usage:

Table 1. Resource Usage

Component Name	Number of Instances
PGA (for gain control)	4
Opamp (for implementing the differentiator)	4
Comparator (for converting the signal to digital)	4
ADC (for implementing the AGC)	1
Analog MUX (for multiplexing the channels)	1 (4-channel)
Number of pins	29 (25 used as analog pins and 4 as digital pins)
RAM	768 bytes
Flash usage	6053 bytes

Figure 9. Schematic

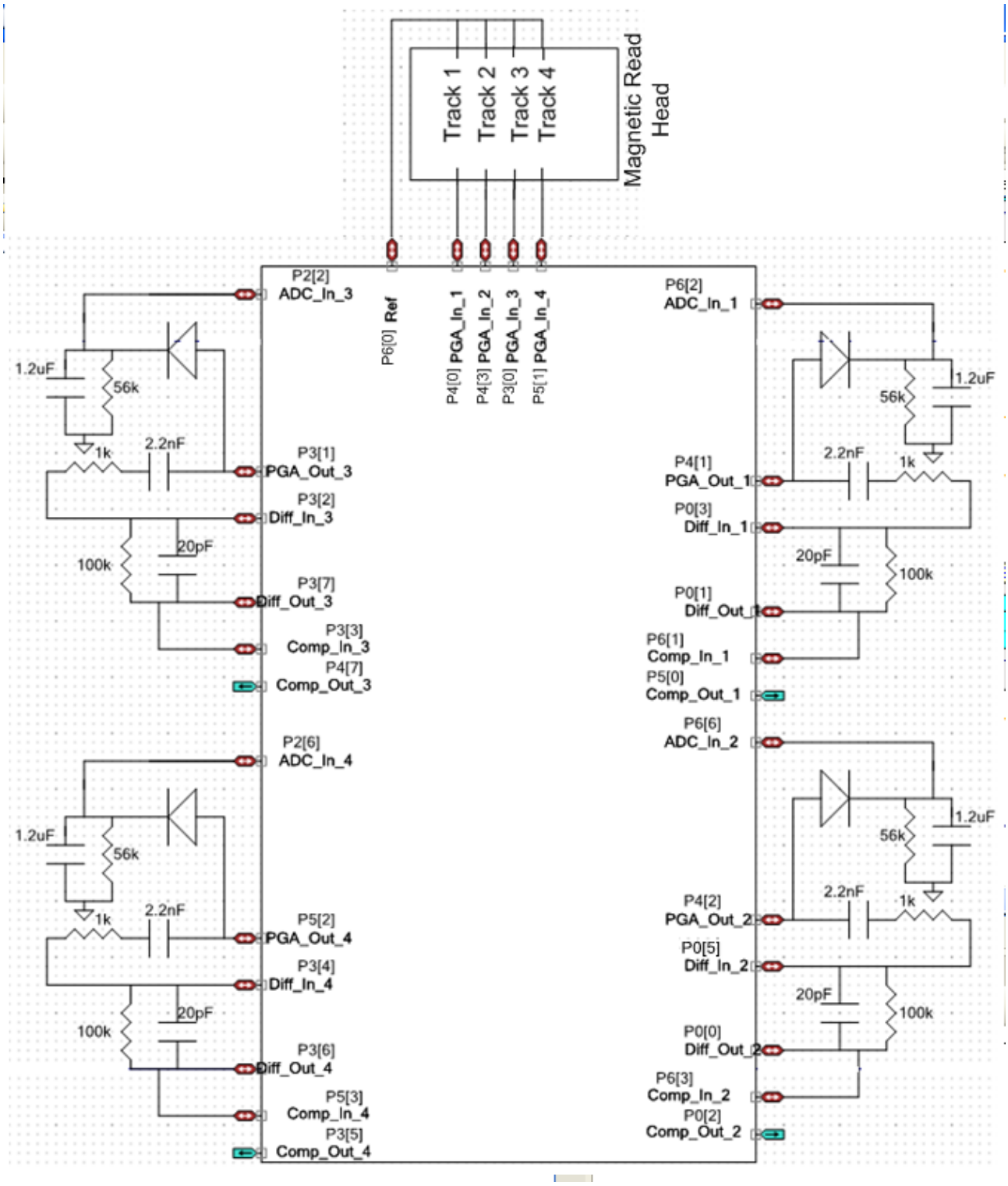


Table 2. Channelwise Pin Placement Summary

Pins	Track1	Track2	Track3	Track4
PGA_In	P4.0	P4.3	P3.0	P5.1
PGA_Out	P4.1	P4.2	P3.1	P5.2
Diff_In	P0.3	P0.5	P3.2	P3.4
Diff_Out	P0.1	P0.0	P3.7	P3.6
Comp_Input	P6.1	P6.3	P3.3	P5.3
Comp_Out	P5.0	P0.2	P4.7	P3.5
ADC_In	P6.2	P6.6	P2.2	P2.6
Reference_Out	P6.0			

Table 3. Bill of Materials

Component	Value	Manufacturer
Resistances	1k, 100k, 56k (4 nos.)	
Diode	Schottky Diode SM5819PL	
Magnetic Read Head	-	SemTek

Summary

PSoC 3 provides enough analog resources and flexible routing ability to implement the four-track magnetic card reader. This application note discusses the design details and waveforms of the MCR along with AGC.

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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2732491	PVKV	07/09/2009	New application note.
*A	2764464	PVKV	09/16/2009	Replaced Figure 8. Updated Table 1. Replaced associated project.

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