

Considerations for the Application of Land Grid Array (LGA) Style Packages

1 Introduction

This application note describes general considerations for application of the Land Grid Array (LGA) style packages.

Freescale has introduced radio frequency (RF) modules such as the MC1320x and MC1321x in LGA packages as an alternative package to ball grid array (BGA).

The LGA packages reduce the amounts of lead in finished products and are Reduction of Hazardous Substances (RoHS) compliant, optimized for improved RF performance for wireless applications and reduce the overall height of the package by eliminating the stand-off height associated with BGA balls. The thinner solder joint also improves thermal dissipation properties compared to BGA packages.

For assistance with any questions about the information contained in this note or for more details about the MC1320x and MC1321x devices, visit www.freescale.com/802154, or contact the appropriate product applications team.

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1.1 Acronyms and Abbreviations

BGA	Ball Grid Array
BT	Bismaleimide Triazine
CBGA	Ceramic Ball Grid Array
CTE	Coefficient of Thermal Expansion
EU	European Union
ESD	Electrostatic Discharge
FR-5	An organic laminate substrate with a relatively high glass transition temperature
HCTE	High Coefficient of Thermal Expansion
HDI	High Density Interconnect
LGA	Land Grid Array
mm	Millimeter
MSL _{<i>n</i>}	Moisture Sensitivity Level <i>n</i>
NSMD	Non-Solder Mask Defined
OSP	Organic Solderability Protectant
PA	Power Amplifier
PCB	Printed Circuit Board
RF	Radio Frequency
RoHS	Reduction of Hazardous Substances
SMD	Solder Mask Defined
SMT	Surface Mount Technology
T _g	Glass Transition Temperature
μm	Micron
White Goods	Home appliances: dishwashers, washers, dryers, refrigerators, etc.

2 LGA RF Module

The LGA package makes the second level interconnect (from package to motherboard) with an array of solderable surfaces. This may consist of a layout similar to a BGA with no solder spheres. However, it may also have an arbitrary arrangement of solderable surfaces that typically includes large planes for grounding or thermal dissipation, smaller lands for signals or shielding grounds, and in some cases, mechanical reinforcement features for mechanical durability.

Freescall has introduced the LGA package using a high coefficient of thermal expansion (HCTE) ceramic in larger body sizes. These are not used in handheld portable applications.

Freescall's product portfolio also includes LGA packages with organic laminate substrates. These feature high density interconnect (HDI) substrates such as bismaleimide triazine (BT) substrates or high-temperature FR-5 style materials. In some cases, an array of joints similar to the BGA may be presented. More often, the lands are square, rectangular, or irregular, as seen in these illustrations of the 34 I/O RF power amplifier module illustrated in HDI 34 Pad RF Power Amplifier Module (Bottom View).

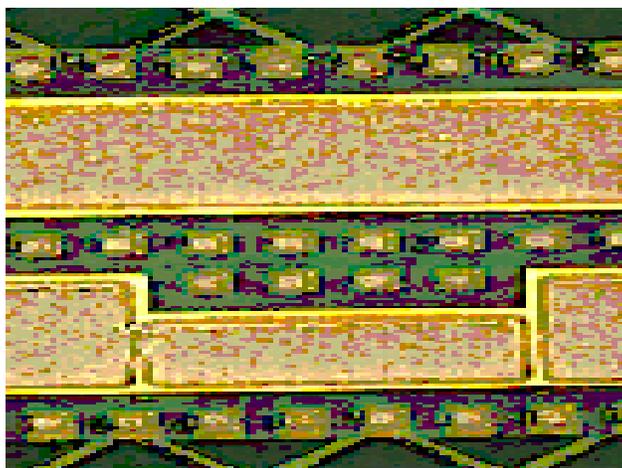


Figure 1. HDI 34 Pad RF Power Amplifier Module (Bottom View)

The physical structure of the package is an organic substrate with patterned conductive traces. The semiconductor devices are mounted on one side of the substrate. The devices are connected to the substrate with either a wire bond or flip chip interconnect. Additional passive devices such as resistors, capacitors, inductors, filters, etc. may also be mounted on the substrate. The devices are then encapsulated with epoxy resin or an equivalent material to provide mechanical and environmental protection to the semiconductors.

The coefficient of thermal expansion (CTE) for the organic alternative substrate materials closely matches the CTE of the PCB materials, ~ 16 ppm/ $^{\circ}\text{C}$. Typically, most epoxy-glass or polyimide-glass PCBs have a CTE of 16-22 ppm/ $^{\circ}\text{C}$. The epoxy resin encapsulation materials have a range of CTE, depending upon the manufacturer, resin system, and filler content. The CTE values are 7-9 ppm/ $^{\circ}\text{C}$ for the Alpha 1 value [below the glass transition temperature (T_g)]. The T_g of the encapsulation materials is typically about 150 $^{\circ}\text{C}$. A cross-section of a typical LGA package may be seen in Cross Section of LGA Module.

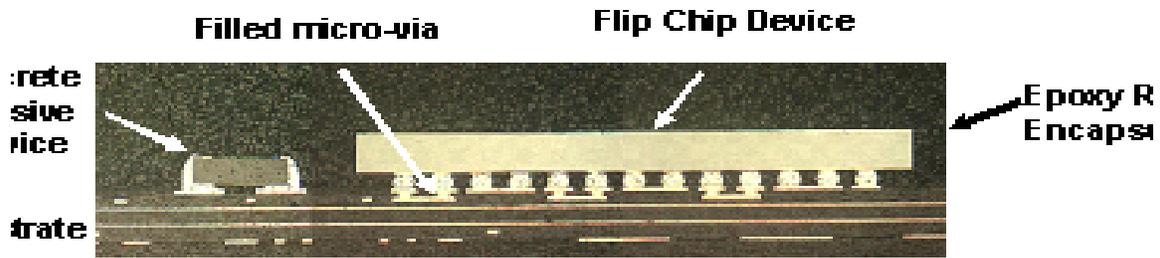


Figure 2. Cross Section of LGA Module

The LGA solder interconnect is formed solely by solder paste applied at board assembly because there are no spheres attached to the LGA. This results in a lower stand-off height of approximately 0.06 mm to 0.10 mm, depending on solder paste volume and printed circuit board (PCB) geometry.

The LGA pad uses the same 0.1 μm to 0.9 μm of electroless gold plating over electroless nickel as has been used reliably for many years in the traditional BGA configuration. LGAs that use a flip chip first level interconnect (from die to package) typically have a 0.15 μm maximum gold thickness. LGAs that have wirebond first level interconnect typically have a 0.5 μm to 0.9 μm gold thickness. Typical Solder Mask Defined (SMD) LGA Pad is an image of a typical LGA pad.

NOTE

LGA lands may be round, square, rectangular, or irregularly shaped, depending on the individual package design.



Figure 3. Typical Solder Mask Defined (SMD) LGA Pad

The only RoHS restricted material in Freescale flip-chip LGA products is lead. These LGA products contain RoHS compliant high-lead bumps between the flip-chip die and substrate as permitted by the RoHS directive Exemption #10, which reads "Lead in high melting temperature type solders (that is, tin-lead solder alloys containing more than 85% lead) and any lower temperature solder required to be used with high melting temperature solder to complete a viable electrical connection." A modified proposed Exemption #10 has been submitted to the European Union (EU) to permit "Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages." Freescale LGA devices can ship under either version of Exemption #10.

Freescale wire bonded LGA products have no lead in them. Lead-free solders and die attach materials are used to attach the integrated circuit device and any discrete passive components within the package to the substrate.

3 Benefits of LGA

Some benefits of the LGA package over a BGA package include:

- LGA devices can be used for either lead containing or lead-free assemblies depending on the surface mount technology (SMT) assembly solder paste used.
- LGA eliminates risk that customers receive components with missing or damaged spheres due to shipping or handling.
- LGA devices have a lower mounted height than BGA. This can allow for more space above the device for a heat sink solution or for small form-factor applications.
- Board-level reliability can significantly exceed customer requirements when the design and process recommendations are followed.
- The durability of LGA in mechanical drop is typically greater than a BGA that is not underfilled.
- LGA can use the same recommended board assembly process as a BGA.

4 LGA Application

The RF module LGAs may be similar in footprint to quad flat no-lead (QFN) packages, especially power amplifier (PA) products. See the Freescale *Quad Flat Pack No-Lead (QFN) Applications Note* (document number: AN1902) for more details.

4.1 Printed Circuit Board Structure

It is recommended that the printed circuit board to which the LGA RF module will be mounted should have a thickness of approximately 1.0 mm or greater. Solder joint stress is strongly effected by the relative thicknesses of the package and the printed circuit board and modeling, which has shown that stress in the solder joint goes up significantly as thicknesses declines below 1.0 mm.

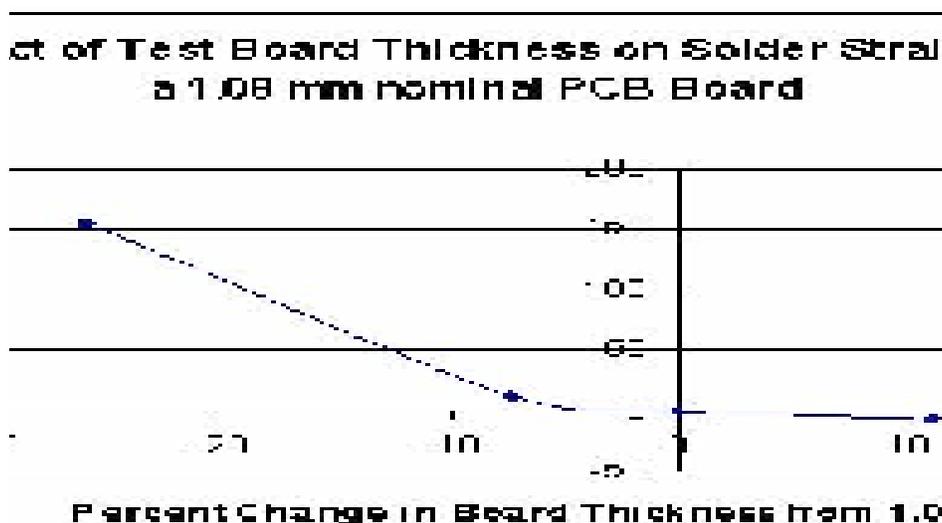


Figure 4. PCB Thickness and Solder Joint Stress

It has also been found that unfilled micro-vias in the mother board or the LGA package will result in solder joint voids. If voids are a concern, then the micro-vias on the mother board and the LGA package should be filled. As shown in [Figure 5](#), the package had filled micro-vias on the LGA package and unfilled micro-vias on the printed circuit void. The voids in evidence are attributable to the unfilled micro-vias on the printed circuit board. [Figure 5](#) shows solder joint voids caused by unfilled PCB micro vias and is taken looking down at the motherboard after the package was removed.



Figure 5. Solder Joint Voids Due to Unfilled Printed Circuit Board Micro-Vias

Unfilled through-vias should not be placed in the solderable areas. The solderable via walls will rob solder from the designed solderable area contributing to voiding and potential opens.

It is recognized that filling the micro-vias requires additional processing and cost in acquiring the package substrate or PCB. The trade-off analysis for the optimum design is most appropriately performed by the customer.

4.2 Land Design

The land design on the mother board should follow the following rules:

- The solderable area on the mother board should match the nominal solderable area on the LGA package 1:1.
- The solderable area should be finished with organic surface protectant (OSP), NiAu, or a solder cladding.
- The decision on whether to have a solder mask defined (SMD) land or a non-solder mask defined (NSMD) land depends on the application space.
- SMD: If field reliability is at risk due to impact failures (dropping a hand-held portable application, such as a cellular telephone, digital camera, MP3 player, etc.) then a SMD land is recommended to optimize mechanical durability.
- NSMD: If field reliability is at risk due to a solder fatigue failure (temperature cycle related open circuits, typically for base station applications, computers, televisions, industrial systems, "white goods", etc.), then a NSMD land is recommended to maximize solder joint life.

The interaction of the various land configurations and via structures is summarized in [Figure 6](#).

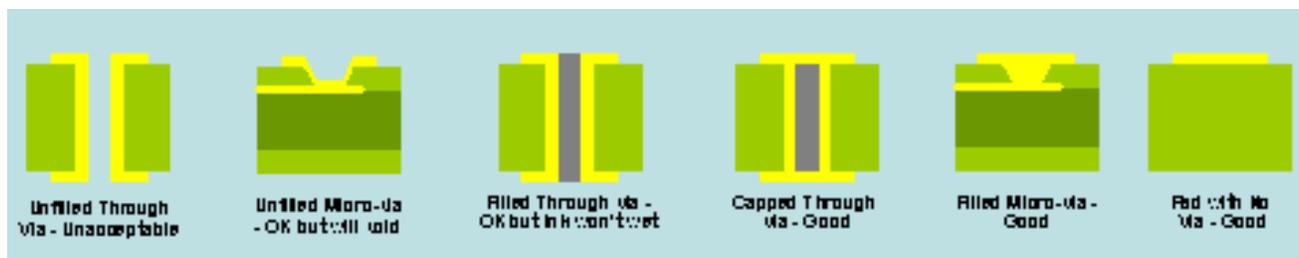


Figure 6. Via Structures and Land Design

4.3 Printed Circuit Board Preparation

Components should be mounted to boards which have just been removed from their dry-pack. If the boards have been exposed to ambient atmosphere longer than the manufacturer's recommendation, then the PCBs may be baked to remove any adsorbed moisture for 4 hours at 125 °C. Customers may have other baking profiles based on their experience or supplier recommendations. Removing moisture prior to reflow is strongly recommended to prevent potential delamination of the PCB during that high temperature excursion.

4.4 Solder Paste Printing

Use automatic equipment to screen print solder paste onto the PCB and a pick and place system to put the RF module LGA package onto the wet solder paste. Typically, an automatic conveyor will take the board into a reflow furnace to solder the components onto the PCB.

Typically, solder paste is applied by automatically dispensing paste through a metal stencil that has been machined to correspond with the pattern of solderable surfaces on the mother board. Freescale has found good results with a 5 mil thick stencil and a 1:1 aperture ratio. Industry practice typically uses stencils from 4 mils to 8 mils in thickness with the thinner stencils typically being associated with finer pitch, more closely spaced application. However, local manufacturing experience may find other combinations of stencil thickness and aperture size, give good results.

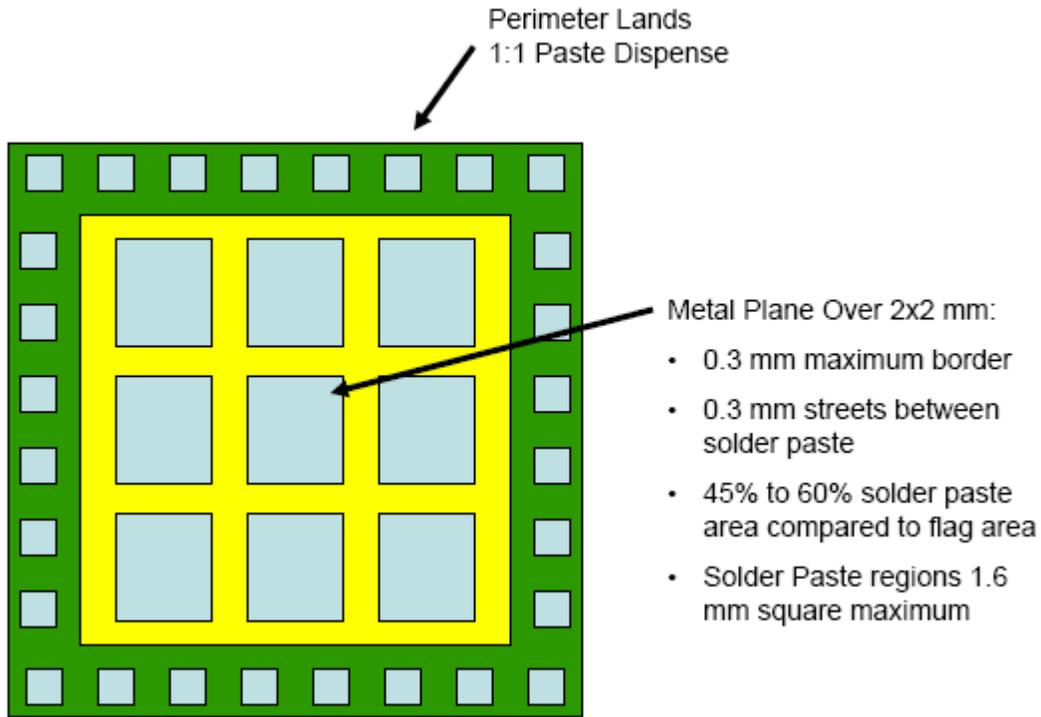
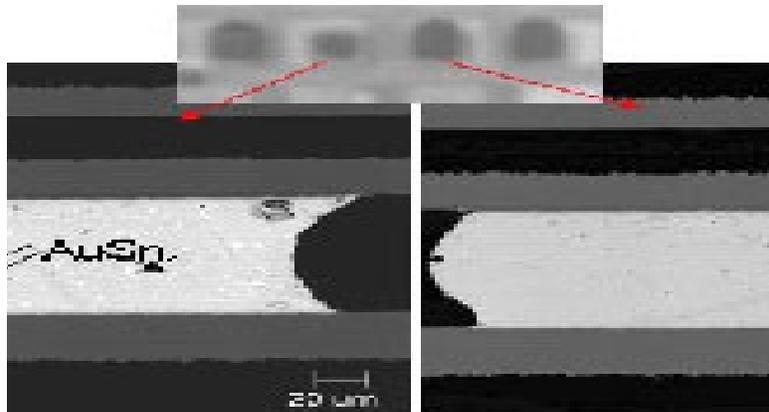


Figure 7. Paste Details

It is strongly recommended that the process should be controlled to maintain a consistent quantity of solder paste on the same sized lands. If a stencil becomes partially blocked (as shown in [Figure 8](#)), then the part may be electrically functional. However, a fragile joint will form. Due to the small quantity of the solder and fixed size and relative thickness of the NiAu metallization, a brittle AuSn₄ intermetallic compound is likely to form. This will result in far less mechanical durability for such a joint than the as-designed nominal solder joint.



**Figure 8. X-Ray Showing Joint With Small Solder Quantity (Top)
Cross-Section Micro-Graph With Affect On Intermetallic Formation and Joint Profile (Bottom)**

Unless otherwise indicated, Freescale studies discussed in this document use Indium no clean NC-SMQ[®] 230 flux and Indalloy[®] 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu. Devices were soldered to boards using the reflow profile illustrated in Reflow for Lead Free Solder Paste”.

4.5 Reflow for Lead Free Solder Paste

Optimal reflow profile depends on solder paste properties and should be optimized and proven out as part of overall process development. The following guidelines for solder reflow represent good soldering practices to help yield high quality assemblies with minimum rework.

It is important to provide a solder reflow profile that matches the solder paste supplier's recommendations. Some fluxes need a long dwell time below the temperature of 180 °C, while others will be burned up in a long dwell time. Temperatures out of bounds of the solder paste flux recommendation could result in poor solderability of all components on the board. All solder paste suppliers should recommend an ideal reflow profile to give the best solderability.

Freescale has achieved good results with Indalloy[®] 241 with a peak temp of 235 °C to 250 °C and a dwell time above 221 °C for greater than 50 seconds and less than 80 seconds as shown in Figure 9.

In IR or convection processes the temperature can vary greatly across the PC board depending on the furnace type, size and mass of components, and the location of components on the PCB. Profiles must be carefully tested to determine the hottest and coolest points on the assembly. The hottest and coolest points should fall within recommended temperatures in the reflow profile. To monitor the process, thermocouples must be carefully attached with very small amounts of thermally conductive grease or epoxy directly to the solder joint interface between the package and board.

4.5.1 Reflow Profile

Figure 9 shows a typical Freescale Pb-free board assembly reflow profile. The example shown is for BGA; however, LGA uses the same profile.

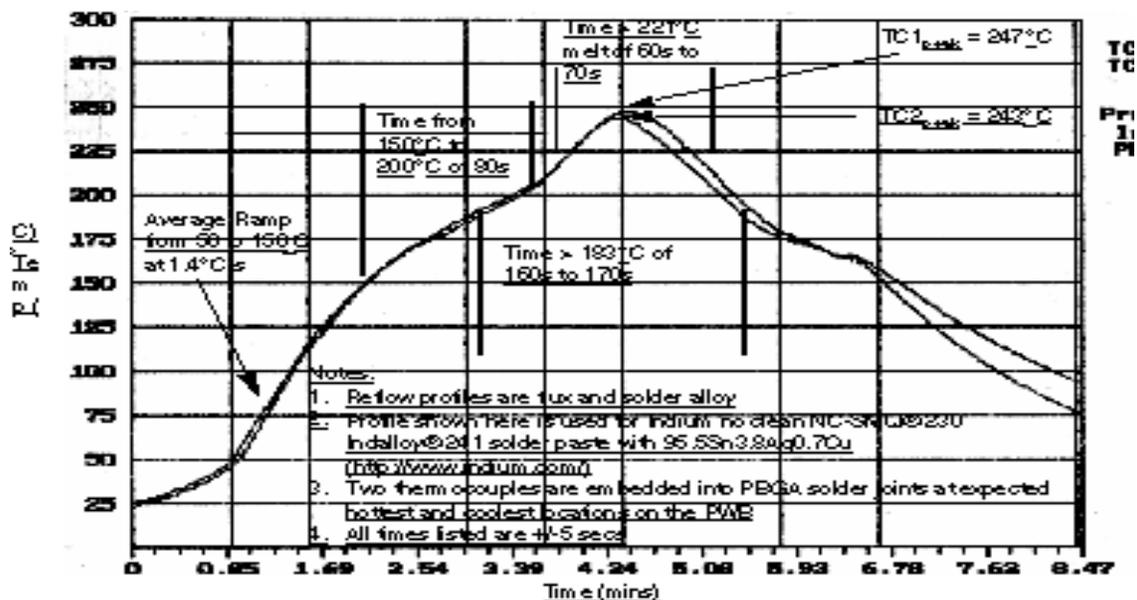


Figure 9. Typical Freescale Pb-Free Board Assembly Reflow Profile

Experience with specific products and production equipment sets may lead users of LGA to have slightly different profiles that are optimized to their local conditions.

4.5.2 Reflow Atmosphere

Assembly and reliability studies were conducted in a furnace with a dry air atmosphere. This setup produces excellent results. However, there are advantages in using a nitrogen atmosphere, such as more complete wetting and a reduction in solder joint voids.

4.5.3 LGA Self Alignment

LGA and BGA array have been shown to be equally tolerant of up to 50% off-pad misplacement. Both package types exhibit self-alignment in any direction including X-axis shift, Y-axis shift, and rotational misplacement. Figure 10 shows device misplacement



Figure 10. LGA Misplacement of 50%

Figure 11 shows a 100% self-aligned soldered down device after 50% misplacement was induced.

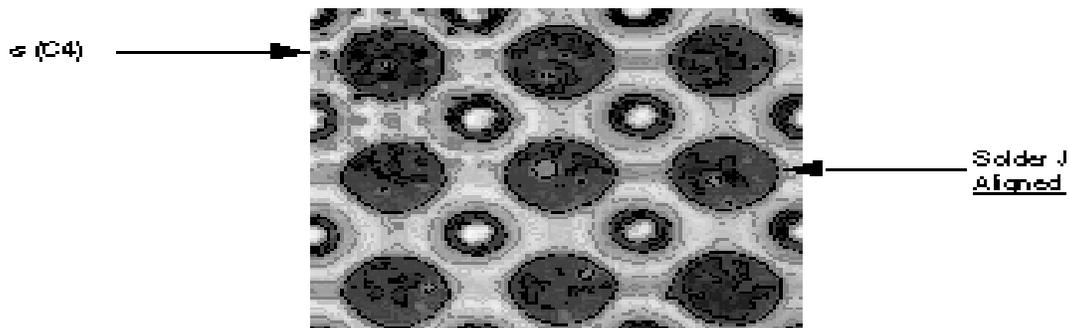


Figure 11. X-ray of Perfectly Self-Aligned LGA After Misplacement

The best experience with self-alignment has been seen with parts that feature arrays of lands. Parts with irregular solderable features on the bottom of the package and large ground planes do not show a strong self-alignment capability. For those packages, it is clear that there is no substitute for careful, precise placement of the component on the PCB.

4.5.4 Cleaning Under LGA

Due to the lower stand-off height of the LGA device, no-clean solder pastes are recommended. Full drying of no-clean paste fluxes as a result of the reflow process must be ensured. This may require longer reflow profiles and/or peak temperatures toward the high end of the process window, as recommended by the solder paste vendor. Instances of uncured flux residues after reflow have been encountered with LGA. It is believed that uncured flux residues could lead to corrosion and/or shorting in accelerated testing and

possibly the field. The presence and extent of uncured flux residues can be detected by mechanical removal of the LGA after reflow as part of the overall assembly development process. Cross-sectioning and flat sectioning are also recommended to assess not only residues, but overall joint geometry.

Solder flux technologies have improved dramatically in recent years, to the point that most of the industry is using no-clean fluxes. Some of these fluxes require specific reflow profiles. The flux vendor's recommendations should always be followed precisely taking precedence over any of the guidelines described in this application note.

Freescale has investigated water soluble solder pastes that do require cleaning in combination with LGA. Using an ion chromatograph, it has been shown that assembly cleanliness is very acceptable, with chlorides detected at $2.11 \mu\text{g}/\text{in}^2$ and bromides at a level of $0.36 \mu\text{g}/\text{in}^2$, following a water clean.

4.6 Handling

Products should be carefully handled at all times in accordance with good electro-static discharge (ESD) procedures to prevent damage to the semiconductor device.

4.7 Rework and Repair

See the Freescale *Land Grid Array Package Rework Applications Note* (document number: AN3281) for more details.

5 LGA Reliability

5.1 Solder Joint Reliability in Temperature Cycling

See the Freescale *Manufacturing with the Land Grid Array Package Applications Note* (document number: AN2920) for more details.

5.2 Mechanical Durability

Performance of packages for mechanical durability, typically through drop testing, depends critically on the thickness of the PCB, the position of the semiconductor component on the PCB, how the PCB is braced within the application, the customer test conditions, the solder joint alloy, and the design of the LGA footprint and surface finish selection.

NOTE

The only variables under Freescale Semiconductor's control are the design and specification of the LGA package. Consult with the application team for any specific package performance information that may be available.

General guidelines which may be used include:

- The size of the package inversely affects its robustness in mechanical durability tests. Small parts are more robust than large parts.

- The typical mechanical durability failure will occur on the corner joints first. Gross failures may open many solder joints. Larger LGA packages may require design features such as increased area on perimeter or corner lands and/or connecting multiple lands into large solderable blocks in order to improve mechanical durability. However, such modifications may obviously affect the package footprint and/or signal routing.
- The pitch of the lands also affects mechanical durability since typically larger LGA pitch results in a larger land solderable area that is more durable. At 1.0 mm pitch, packages up to 11 x 15 mm have demonstrated satisfactory mechanical durability. At 0.8 mm pitch, packages up to 9 x 11 mm have demonstrated satisfactory durability. At 1.0 mm and 0.8 mm pitch, it appears that there is still some additional package size that could be accommodated without undue adverse effect on the mechanical durability. At 0.65 mm pitch, the maximum package size with corner reinforcement appears to be about 8 x 8 mm maximum. This is clearly a case where individual designs can be adjusted to optimize mechanical durability. Also, if the product application space is outside of the area where impact resistance is critical to field reliability, then these package size concerns do not apply. If there is any question consult your product application team on specific products.
- The location of the package in the application strongly affects its robustness. Improved mounting/bracing of a printed circuit board within the application can help. Redesign of the printed circuit board to move the semiconductor package to a location with less mechanical stress or increasing the thickness of the mother board for greater rigidity can help.

A more rigid PCB, all other things being equal, will reduce the stress in the solder joints and improve mechanical durability. The greater PCB rigidity is typically achieved by increasing the PCB thickness. Modeling predicts that solder joint stress increases in a non-linear fashion with decreasing PCB board thickness. Therefore, a 20% reduction in board thickness will result in a much greater than 20% increase in solder joint stress. See [Section 5.1, “Solder Joint Reliability in Temperature Cycling”](#).

“Slotting” of the mother board to reduce mechanical stress (as taught in US Patent 6,160,713A) may also be used upon licensing the art disclosed in that patent. See [Figure 12](#). Label 110 is the PCB. Label 108 is the array of lands to receive a semiconductor package on the PCB. Label 202 is a slot in the PCB.

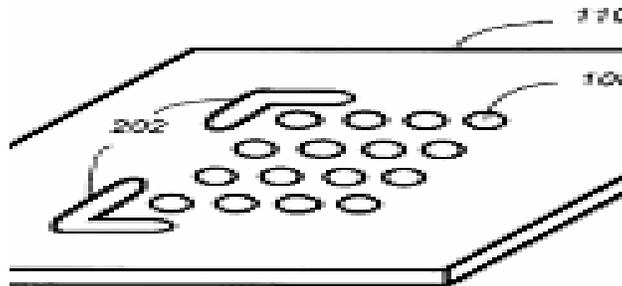


Figure 12. Slotted PCB Board Innovation

- The application should drive the PCB land construction details. NSMD lands on the PCB are known to give better temperature cycling reliability [See the Freescale *Manufacturing with the Land Grid Array Package Applications Note* (document number: AN2920) for more details.]. However, Freescale has found that SMD pads improve the mechanical durability compared to NSMD pads in drop testing. A PCB land configuration should be selected based on assessments of

the product, bearing in mind the general application space. Freescale has observed a greater sensitivity to mechanical durability in drop testing for some market segments such as cell phones, portable music players, flash memory, etc. Other business segments such as computers, servers, and base stations emphasize good performance with respect to temperature cycling fatigue.

6 References

Quad Flat Pack No-Lead (QFN) Applications Note (document number: AN1902)

Manufacturing with the Land Grid Array Package Applications Note (document number: AN2920)

Land Grid Array Package Rework Applications Note (document number: AN3281)

U.S. Patent 6,160,713A

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