Power tip: Cut transformer interwinding capacitance effects

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If you have already built a low-power flyback converter with a high turns ratio, you have most likely faced problems with interwinding capacitance. In this article, we take a look at techniques to reduce the capacitance effects that allow higher frequency operation.

Figure 1 illustrates a circuit that is indicative of the problem. In this transformer, we started with a high turns ratio (40:1) between the secondary and the primary windings.

The transformer has distributed capacitance from the secondary winding-to-ground. The high-voltage switching on the secondary causes current to flow in this capacitance, which is reflected back to the primary. The effective capacitance seen on the primary is the secondary distributed capacitance multiplied by the turns ratio squared.

For instance, 20 pF of distributed capacitance is multiplied by 1600. This appears as 32 nF of capacitance on the primary and generates significant loss. At 100 kHz and 12 volt input, for example, the loss attributed to this capacitance is equal to almost 1 watt in this 4 watt power supply. This capacitance slows the drain voltage as the power FET turns off, robbing you of duty factor. It can also cause false triggering of current limits when the MOSFET turns on.

The secret to reducing current that flows through the capacitance is to minimize the transformer-turns ratio and minimize the voltage across it. There are a number of ways to minimize the voltage. Typically, in these high-voltage circuits, the windings are wound in layers. With two layers, when the end and start are on the same side of the bobbin, the first and last turns have the full winding voltage between them.

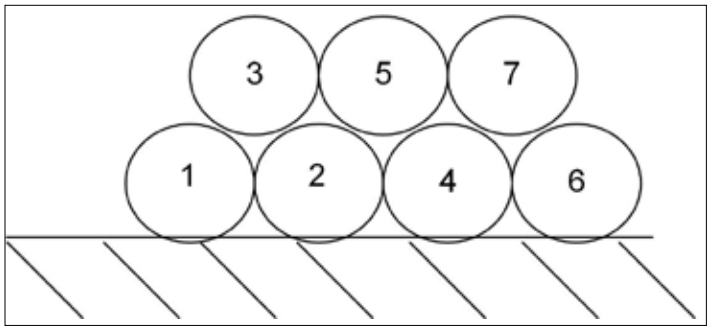

Figure 2: Bank winding reduces effective capacitance.

One technique used to reduce the gradient between the turns is called bank winding. The wires are wound as shown in **figure 2**. This method can significantly reduce the capacitance by limiting the voltages between the adjacent windings. Winding in sections with a split bobbin is an extension of this method.

If the transformer capacitance is still an issue, there are some circuit tricks that you can play. **Figure 3** shows an example.

In this design we have split the secondary windings so that they provide half the voltage of the secondaries shown in figure 1, but we have connected two of them in series for each output. The average AC voltage on the lower-voltage winding remains

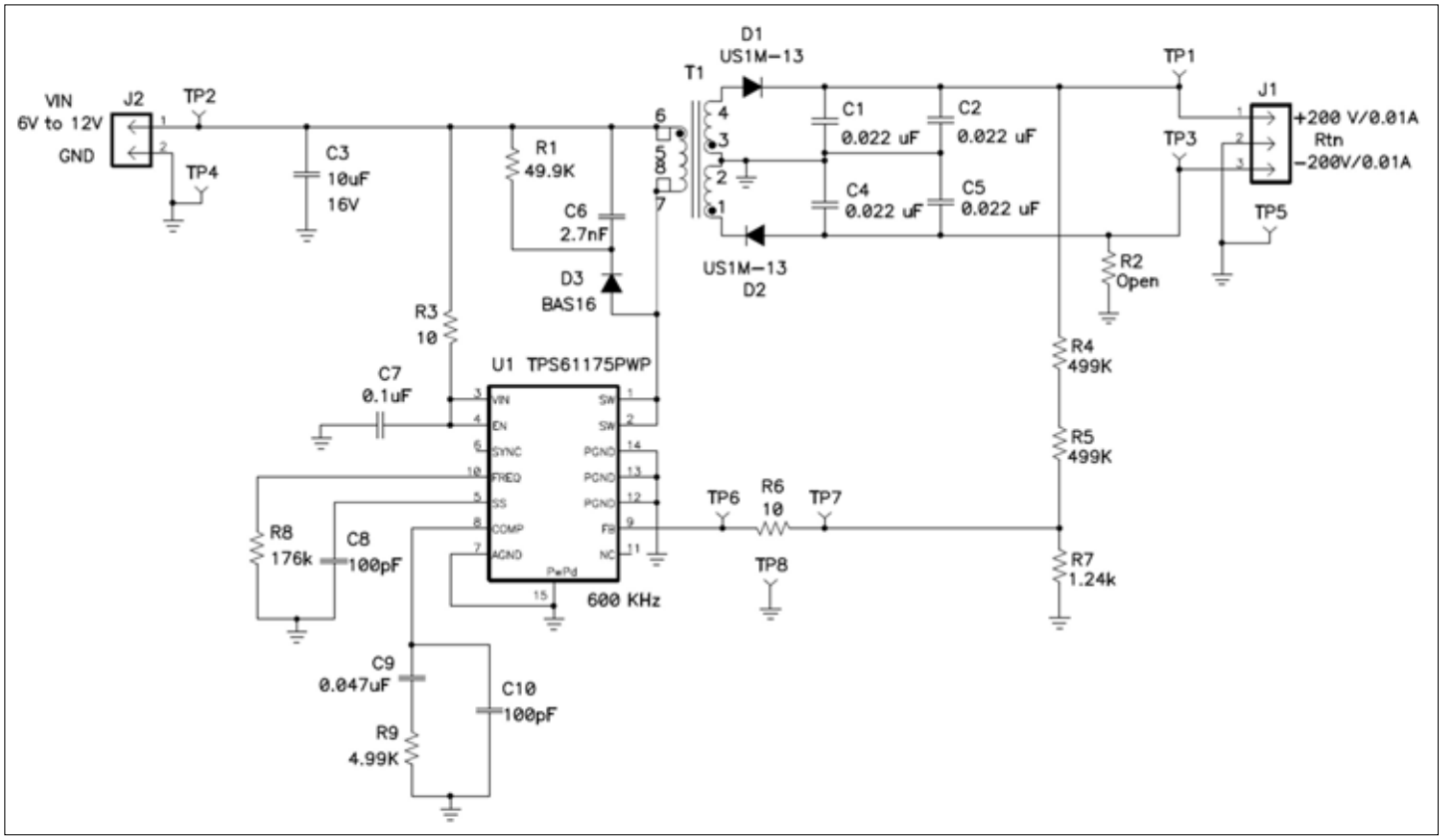

Figure 1: Interwinding capacitance is problematic with high transformer-turn ratio.

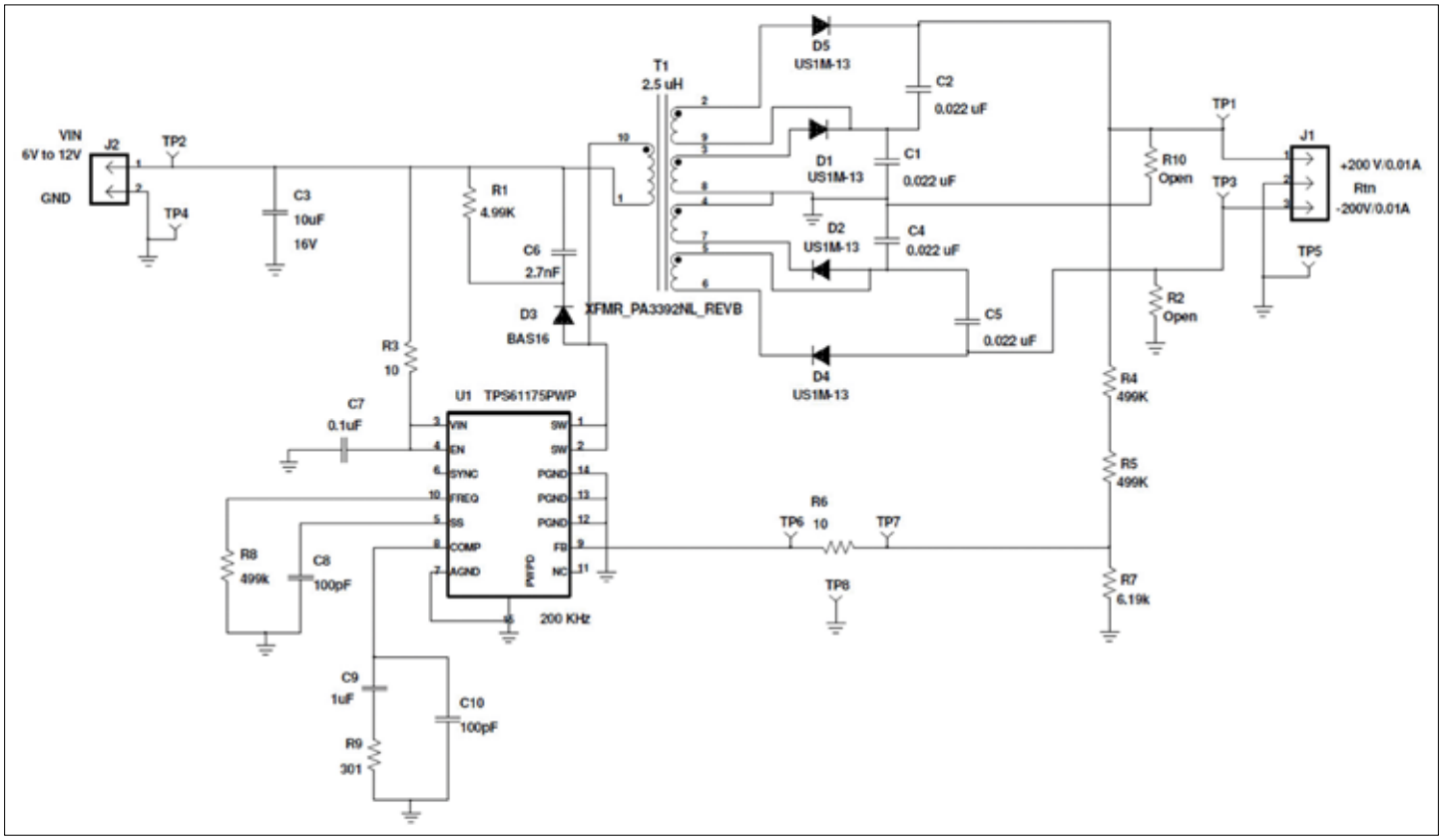

Figure 3: Splitting secondary can halve distributed capacitance.

the same, while the average AC voltage on the higher winding is reduced by 66 percent. This method reduces the effective transformer capacitance by about half, and can be extended to more sections for even higher voltages.

To summarize, interwinding capacitance can be a problem where large transformer-turns ratios are involved, particularly with low-power converters where losses can be a significant percentage of the load power. The secret to a low-capacitance transformer design is to minimize the turns ratio and to minimize the voltage across adjacent windings.

This can be accomplished by bank, or section windings. You can also split the windings and add rectifiers and filters to further reduce the capacitance. The effective capacitance will be reduced by the number of sections. For instance, four sections reduce capacitance by a factor of four.