Freescale Semiconductor
Application Note

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Common Hardware Design for i.MX 6Dual/6Quad and i.MX 6Solo/6DualLite

The i.MX 6Quad, i.MX 6Dual, i.MX 6DualLite, and i.MX 6Solo families of applications processors represent Freescale Semiconductor's ARM Cortex™-A9 based multimedia-focused products that offer high performance processing with a high degree of functional integration and are optimized for low power consumption.

The i.MX 6Dual/6Quad and i.MX 6Solo/6DualLite processors have similar features and implementation. Their similar implementation makes possible the hardware migration of these processors from one processor type to another. This application note explains how to achieve a common hardware design for i.MX 6Dual/6Quad and i.MX 6Solo/6DualLite.

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1 Overview

The i.MX 6Quad, i.MX 6Dual, i.MX 6DualLite, and i.MX 6Solo families of applications processors feature Freescale's advanced implementation of the quad/dual/solo ARM Cortex-A9 core. They include 2D and 3D graphics processors, 3D 1080p video processing, and integrated power management. Each processor provides a DDR3/LV-DDR3/LPDDR2 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

They can be used in a variety of applications such as:

- Automotive infotainment
- eReaders
- Human-machine interface
- Home energy management systems
- In-flight entertainment
- Intelligent industrial control systems
- IP phones
- IPTV
- Portable medical
- Smartbooks
- Tablets

Note that each processor has a part family, meaning that there are multiple versions of each part with the possibility of different features/modules enabled or disabled in each version. Each part in the family targets a specific market segment (consumer, automotive, or industrial). For a complete list of currently available part versions and their included features/modules, see the latest chip-specific data sheet.

2 Common features

The i.MX 6Quad, i.MX 6Dual, i.MX 6DualLite, and i.MX 6Solo processors contain a number of digital and analog modules. For a more detailed description of all of the modules and features of each processor, see the chip-specific data sheet and reference manual.

Table 1 shows the common features of these four processors. Hardware design of the common features should be the same for all the processors.

Table 1. Summary of common features

Features	Description
NAND Flash	8 bit, support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™, and others. BCH ECC up to 40 bit.
NOR Flash	16/32 bit, all EIMv2 signals are muxed on other interfaces
PSRAM	16/32 bit, Cellular RAM
Parallel display port	24 bit, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
HDMI TX	Supports HDMI TX 1.4

Table 1. Summary of common features (continued)

Features	Description
Parallel camera port	Supports up to 20 bit and up to 240 MHz peak
MMC/SD/SDIO	Four MMC/SD/SDIO card ports all supporting: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
USB	One High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY Three USB 2.0 (480 Mbps) hosts: • One HS host with integrated High Speed PHY • Two HS hosts with integrated HS-IC USB (high speed interchip USB) PHY
PCIe	Support V2.0 one lane • PCI Express (Gen 2.0) dual mode complex, supporting root complex operations and endpoint operations. Uses x1 PHY configuration.
I2S/SSI/AC97	Up to 1.4 Mbps each
ESAI	Up to 1.4 Mbps per channel
UART	Five UARTs, up to 4.0 Mbps each: • Providing RS232 interface • Supporting 9-bit RS485 multidrop mode • One of the five UARTs supports 8-wire while other four support 4-wire
Gigabit Ethernet controller	IEEE1588 compliant, 10/100/1000Mbps
PWM	Four pulse width modulators
SJC	System JTAG controller
GPIO	With interrupt capabilities
KPP	8x8 keypad port
SPDIF	Sony Philips Digital Interface, Rx and Tx
FlexCAN	Two controller area networks (FlexCAN), 1 Mbps each
WDOG	Two watchdog timers (WDOG)
AUDMUX	Audio MUX
LVDS	One port up to 165 Mpixels/sec or two ports up to 85 Mpixels/sec (for example, WUXGA at 60 Hz) each

3 Feature differences

Table 2 shows feature differences for the i.MX 6Quad, i.MX 6Dual, i.MX 6DualLite, and i.MX 6Solo processors.

Table 2. Summary of feature differences

Features	i.MX 6Quad	i.MX 6Dual	i.MX 6DualLite	i.MX 6Solo
Core	Quad Cortex-A9	Dual Cortex-A9	Dual Cortex-A9	Solo Cortex-A9
Memory (1-channel)	Up to 4 GB, x16/x32/x64 for • DDR3-1066 • LV-DDR3-1066 • LPDDR2-1066	Up to 4 GB, x16/x32/x64 for • DDR3-1066 • LV-DDR3-1066 • LPDDR2-1066	Up to 4 GB, x16/x32/x64 for • DDR3-800 • LV-DDR3-800 • LPDDR2-800	Up to 4 GB, x16/x32 for • DDR3-800 • LV-DDR3-800 • LPDDR2-800
Memory (2-channel)	Up to 4 GB, LPDDR2-1066 • 2x32/channel • Four chip select signals (two signals/channel) • Supports DDR interleaving mode	Up to 4 GB, LPDDR2-1066 • 2x32/channel • Four chip select signals (two signals/channel) • Supports DDR interleaving mode	Up to 4 GB, LPDDR2-800 • 2x32/channel • Four chip select signals (two signals/channel) • Supports DDR interleaving mode	—
RAM	256 KB	256 KB	128 KB	128 KB
L2 cache	1 MB unified I/D L2 cache, shared by quad core	1 MB unified I/D L2 cache, shared by dual core	512 KB unified I/D L2 cache, shared by dual core	512 KB unified I/D L2 cache
IPU	Two autonomous and independent IPUs	Two autonomous and independent IPUs	One IPU	One IPU

Graphics acceleration	Three independent, integrated graphics processing units:
	• OpenGL® ES 2.0 3D graphics accelerator with four shaders
	  • Up to 200 MT/s
	  • OpenCL support
	• 2D graphics accelerator
	• Dedicated OpenVG™ 1.1 accelerator
		Three independent, integrated graphics processing units:
		• OpenGL® ES 2.0 3D graphics accelerator with four shaders
		  • Up to 200 MT/s
		  • OpenCL support
		• 2D graphics accelerator
		• Dedicated OpenVG™ 1.1 accelerator
			Two independent, integrated graphics processing units:
			• OpenGL® ES 2.0 3D graphics accelerator with one shader
			• 2D graphics accelerator
				Two independent, integrated graphics processing units:
				• OpenGL® ES 2.0 3D graphics accelerator with one shader
				• 2D graphics accelerator

Electrophoretic Display (EPD) Controller	—	—	Supports E-INK color and monochrome • Up to 1650x2332 resolution • Up to 5-bit grayscale (32-levels per color channel)	Supports E-INK color and monochrome • Up to 1650x2332 resolution • Up to 5-bit grayscale (32-levels per color channel)

Table 2. Summary of feature differences (continued)

Features	i.MX 6Quad	i.MX 6Dual	i.MX 6DualLite	i.MX 6Solo
Displays	Supports: • Parallel display • HDMI1.4 • MIPI display • Two LVDS displays • Up to four displays at a time.	Supports: • Parallel display • HDMI1.4 • MIPI display • Two LVDS displays • Up to four displays at a time.	Supports: • Parallel display • HDMI1.4 • MIPI display • Two LVDS displays • Up to two displays at a time.	Supports: • Parallel display • HDMI1.4 • MIPI display • Two LVDS displays • Up to two displays at a time.
Video input	Supports three video inputs	Supports three video inputs	Supports two video inputs	Supports two video inputs
MIPI camera	Supports four lanes	Supports four lanes	Supports two lanes	Supports two lanes
SATA	SATAII, 3.0 Gbps	SATAII, 3.0 Gbps	—	—
I^2C	Three I^2C, supporting 400 kbps	Three I^2C, supporting 400 kbps	Four I^2C, supporting 400 kbps	Four I^2C, supporting 400 kbps
eCSPI	Five eCSPI	Five eCSPI	Four eCSPI	Four eCSPI

4 Hardware requirements for migration

4.1 Connection differences

These i.MX 6 series devices use the same pinouts, with the exception of the power signals and specific features discussed in this section.

CAUTION

The i.MX 6Dual/6Quad and i.MX 6Solo/6DualLite hardware designs are not exactly same, rather have some significant connection differences. So, before starting a common hardware design, the user need to understand well the connection differences between the two hardware designs.

The first connection difference between the i.MX 6Dual/6Quad and i.MX 6Solo/6DualLite hardware designs is how to connect the VDDARMxx_xx power domain. Table 3 explains how this power domain should be connected in each device. As shown in Table 3, the VDDARM_IN and VDDARM_CAP domains use the same connections for all the devices.

Table 3. VDDARMxx_xx connections

Domain name	i.MX 6Quad	i.MX 6Dual	i.MX 6Solo/6DualLite
VDDARM23_IN	Connect to power supply (K9, L9, M9, N9, P9, R9, T9, U9)	Connect to GND (K9, L9, M9, N9, P9, R9, T9, U9)	VDDARM23_IN is not defined in i.MX 6DualLite and i.MX 6Solo. All power pins are defined as VDDARM_IN.
VDDARM23_CAP	Place external capacitors (H11, J11, K11, L11, M11, N11, P11, R11)	Connect to GND (H11, J11, K11, L11, M11, N11, P11, R11)	VDDARM23_CAP is not defined in i.MX 6DualLite and i.MX 6Solo. All power pins are defined as VDDARM_CAP.
VDDARM_IN	Connect to power supply (H14, J14, K14, L14, M14, N14, P14, R14)	Connect to power supply (H14, J14, K14, L14, M14, N14, P14, R14)	Connect to power supply (H14, J14, K9, K14, L9, L14, M9, M14, N9, N14, P9, P14, R9, R14, T9, U9)
VDDARM_CAP	Place external capacitors (H13, J13, K13, L13, M13, N13, P13, R13)	Place external capacitors (H13, J13, K13, L13, M13, N13, P13, R13)	Place external capacitors (H11, H13, J11, J13, K11, K13, L11, L13, M11, M13, N11, N13, P11, P13, R11, R13)

CAUTION

Note that in an i.MX 6Quad hardware design, VDDARM23_CAP must be connected to VDDARM_CAP; otherwise, inner cores may get damaged.

The second difference is that these devices support different EIM power rails. The i.MX 6Quad and i.MX 6Dual support three different EIM power rails:

- NVCC_EIM0(K19)
- NVCC_EIM1(L19)
- NVCC_EIM2(M19)

Unlike the i.MX 6Quad and i.MX 6Dual, the i.MX 6DualLite and i.MX 6Solo support only one EIM power rail, NVCC_EIM(K19, L19, M19). The three power pins must be connected to the same power supply.

The third difference is about VDD_CACHE_CAP (N12). In i.MX 6Quad and i.MX 6Dual, VDD_CACHE_CAP should be connected to VDDSOC_CAP, whereas in i.MX 6DualLite and i.MX 6Solo, pin N12 can be NC.

The fourth difference is about SATA_VP (G13) and SATA_VPH (G12). In i.MX 6Quad and i.MX 6Dual, SATA_VP and SATA_VPH are recommended to be grounded, if not in use. In i.MX 6DualLite and i.MX 6Solo, no SATA function is available and all these pins are recommended to be NC.

4.2 All-In-One circuit

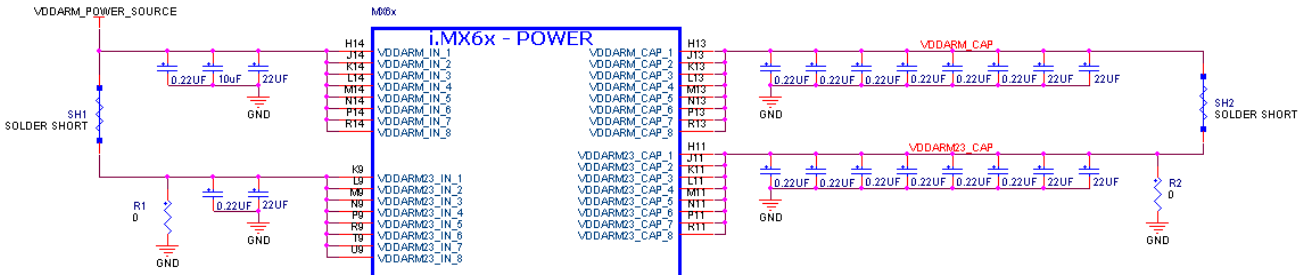


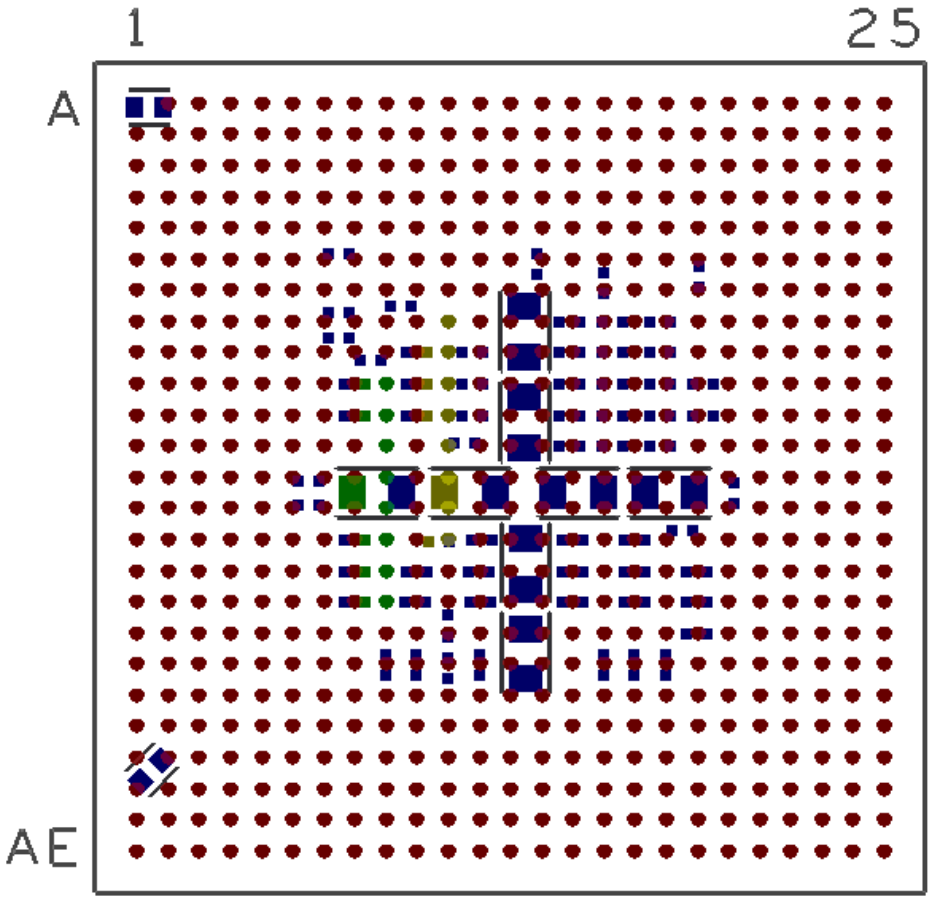
Figure 1. All-In-One circuit

Table 4. VDDARMxx_xx Power Connections

	i.MX 6Quad	i.MX 6Dual	i.MX 6DualLite	i.MX 6Solo
SH1	Shorted	Open	Shorted	Shorted
SH2	Shorted	Open	Shorted	Shorted
R1	Open	Shorted	Open	Open
R2	Open	Shorted	Open	Open

4.3 Capacitor placement

It is highly recommended that the user places the decoupling and bulk capacitors of the power domains on the bottom layer of the hardware design, directly underneath the associated package contacts. Figure 2 shows the recommended placement for the VDDARMxx_xx domains. For detailed design information, see *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (IMX6DQ6SDLHDG).



Legend

Red	i.MX 6x on top layer
Blue	Capacitor footprints at bottom layer
Green	VDDARMxx_IN
Yellow	VDDARMxx_CAP

Figure 2. Decoupling capacitor placement

5 DRAM interface requirements for migration

All these chips support up to 4 Gbyte DDR memory space. Since the i.MX 6Dual, i.MX 6Quad, and i.MX 6DualLite have the same ball map, they have similar DRAM PCB layout routing. However, the i.MX 6Solo supports only 32-bit DRAM; therefore, signals D32~D63, DQM4~7, and SDQS4~7 (_B) can be NC.

5.1 DDR3 connections

The following table summarizes the differences in the chip DDR3 connections.

Table 5. Summary of differences in DDR3 support

Device	DDR3 support
i.MX 6Quad	16/32/64-bit • DDR3-1066 • LV-DDR3-1066
i.MX 6Dual	16/32/64-bit • DDR3-1066 • LV-DDR3-1066
i.MX 6DualLite	16/32/64-bit • DDR3-800 • LV-DDR3-800
i.MX 6Solo	16/32-bit • DDR3-800 • LV-DDR3-800

5.1.1 64-bit, two chip selects DDR3 use case

In the 64-bit, two chip selects use case, when migrating the i.MX 6Dual/6Quad hardware design to the i.MX 6DualLite, the only hardware change is that the memory access speed will be reduced. In this use case, when migrating the i.MX 6Dual/6Quad hardware design to the i.MX 6Solo, the four DDR3 devices in the upper 32 bits may not be populated (DNP), but this will leave layout stubs that may affect DDR3 performance. Ideally, the layout should be modified to remove these stubs.

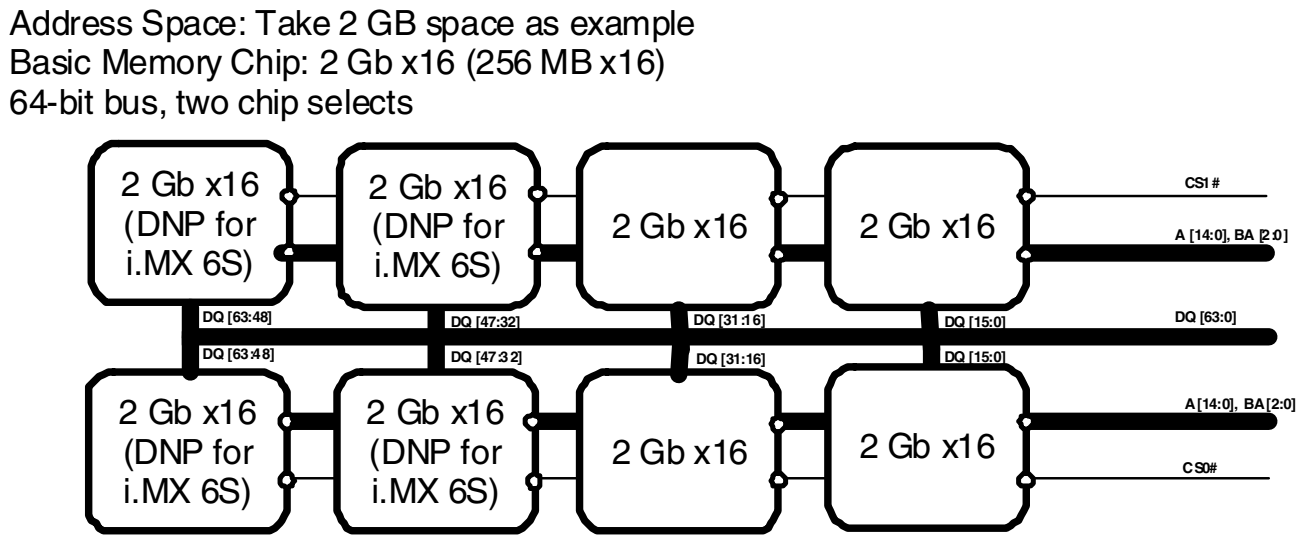


Figure 3. 64-bit, two chip selects DDR3 use case

5.1.2 64-bit, one chip select DDR3 use case

In the 64-bit, one chip select use case, when migrating the i.MX 6Dual/6Quad hardware design to the i.MX 6DualLite, no hardware change is needed except that the memory access speed will be reduced. In this use case, when migrating the i.MX 6Dual/6Quad hardware design to the i.MX 6Solo, the two DDR3 devices in the upper 32 bits may not be populated (DNP), but this will leave layout stubs that may affect DDR3 performance. Ideally, the layout should be modified to remove these stubs.

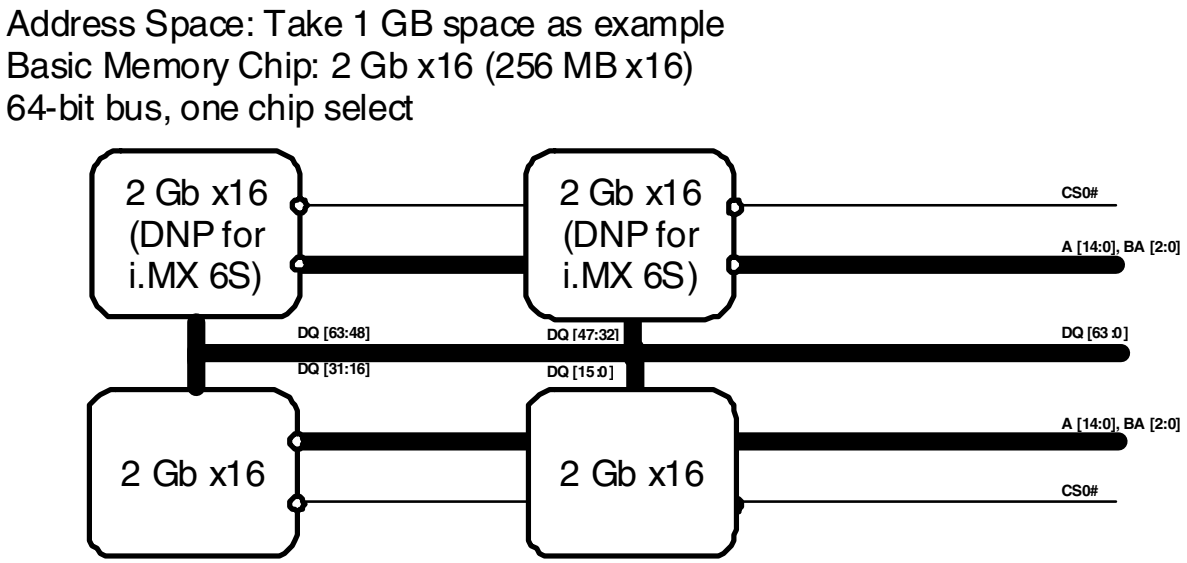


Figure 4. 64-bit, one chip select DDR3 use case

5.1.3 32-bit, two chip selects DDR3 use case

In the 32-bit, two chip selects use case, when migrating the i.MX 6Dual/6Quad hardware design to the i.MX 6Solo/6DualLite, no hardware change is needed except that the memory access speed will be reduced.

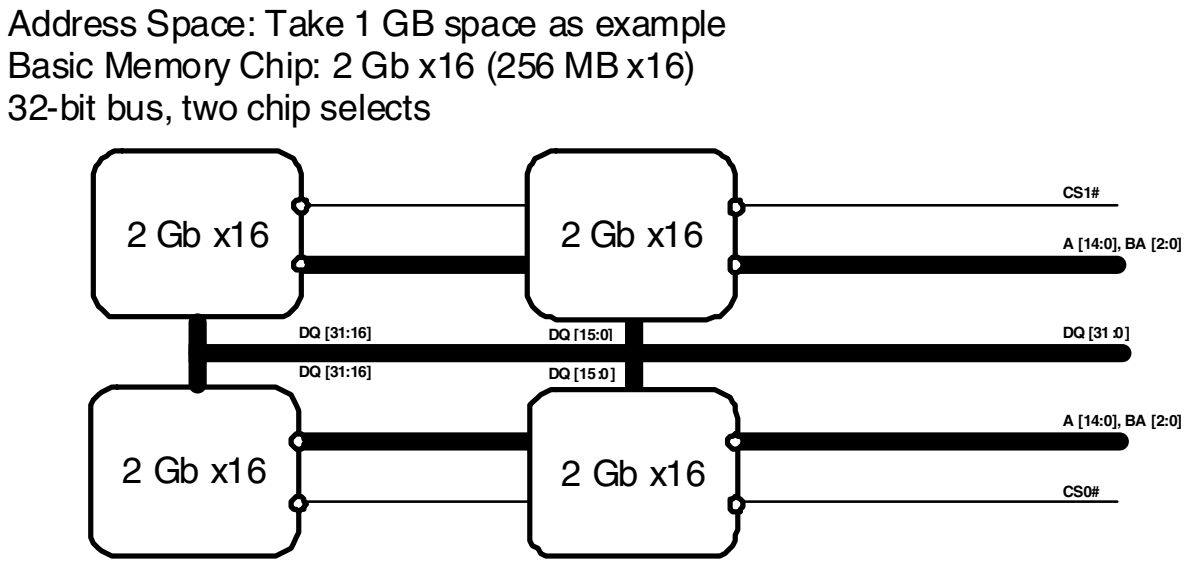


Figure 5. 32-bit, two chip selects DDR3 use case

NOTE

In each use case, the designer can swap the data sequence within a byte for easy routing or pinout, except for the lowest bit of each byte that will be used for hardware write leveling calibration.

5.2 LPDDR2 connections

The following table summarizes the differences in the chip LPDDR2 connections.

Table 6. Summary of differences in LPDDR2 support

Device	LPDDR2 support
i.MX 6Quad	LPDDR2-1066 • 16/32/64-bit • 2×32 configuration
i.MX 6Dual	LPDDR2-1066 • 16/32/64-bit • 2×32 configuration
i.MX 6DualLite	LPDDR2-800 • 16/32/64-bit • 2×32 configuration
i.MX 6Solo	LPDDR2-800 • 16/32-bit

5.2.1 64-bit, dual channel LPDDR2 use case

The 64-bit, dual LPDDR2 (interleave) use case works for three devices:

- i.MX 6Quad
- i.MX 6Dual
- i.MX 6DualLite

Address Space: Take 1 GB space as example
Basic Memory Chip: 1 GB, dual channel, x32

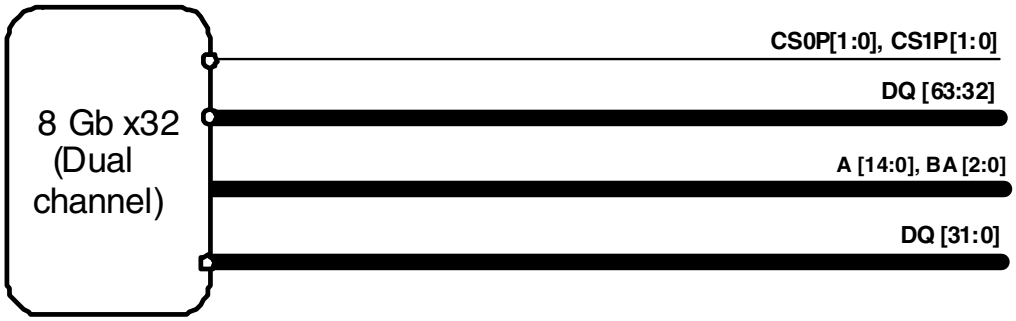


Figure 6. 64-bit LPDDR2 connection

6 EPD controller requirements for migration

The i.MX 6Dual and i.MX 6Quad processors do not have an Electrophoretic Display (EPD) Controller (but the i.MX 6Solo and i.MX 6DualLite processors do), hence the designer has to reserve the EPD related signals when migrating an i.MX 6Quad or i.MX 6Dual hardware design to the i.MX 6DualLite or i.MX 6Solo for an eReader application.

Table 7 shows how the i.MX 6DualLite and i.MX 6Solo EPD muxed signals are muxed with EIM signals.

Table 7. EPD muxed signals

Contact name	Mux mode ALT 8
EIM_DA14	epdc.SDDO[14]
EIM_DA15	epdc.SDDO[9]
EIM_BCLK	epdc.SDCE[9]
EIM_DA13	epdc.SDDO[13]
EIM_DA10	epdc.SDDO[1]
EIM_DA12	epdc.SDDO[2]
EIM_DA9	epdc.SDCE[5]
EIM_DA11	epdc.SDDO[3]
EIM_DA7	epdc.SDCE[3]
EIM_DA5	epdc.SDCE[1]
EIM_DA8	epdc.SDCE[4]
EIM_DA4	epdc.SDCE[0]
EIM_DA2	epdc.BDR[0]
EIM_DA6	epdc.SDCE[2]
EIM_DA0	epdc.SDCLKN
EIM_DA3	epdc.BDR[1]
EIM_EB1	epdc.SDSHR
EIM_EB0	epdc.PWRCOM
EIM_DA1	epdc.SDLE
EIM_LBA	epdc.SDDO[4]
EIM_OE	epdc.PWRIRQ
EIM_RW	epdc.SDDO[7]
EIM_CS1	epdc.SDDO[8]
EIM_A16	epdc.SDDO[0]
EIM_A18	epdc.PWRCTRL[0]
EIM_CS0	epdc.SDDO[6]
EIM_A23	epdc.GDOE

Table 7. EPD muxed signals (continued)

Contact name	Mux mode ALT 8
EIM_A21	epdc.GDCLK
EIM_A19	epdc.PWRCTRL[1]
EIM_A20	epdc.PWRCTRL[2]
EIM_A24	epdc.GDRL
EIM_A17	epdc.PWRSTAT
EIM_A22	epdc.GDSP
EIM_D26	epdc.SDOED
EIM_D28	epdc.PWRCTRL[3]
EIM_D30	epdc.SDOEZ
EIM_D23	epdc.SDDO[11]
EIM_D31	epdc.SDCLK
EIM_D18	epdc.VCOM[1]
EIM_D25	epdc.SDCE[8]
EIM_EB3	epdc.SDCE[0]
EIM_D16	epdc.SDDO[10]
EIM_D29	epdc.PWRWAKE
EIM_D27	epdc.SDOE
EIM_D19	epdc.SDDO[12]
EIM_A25	epdc.SDDO[15]
EIM_D24	epdc.SDCE[7]
EIM_D22	epdc.SDCE[6]
EIM_D17	epdc.VCOM[0]
EIM_EB2	epdc.SDDO[5]

7 Display feature differences

The figures in this section show the differences in the display setups for the different chips. Note the following:

- The i.MX 6Quad and i.MX 6Dual chips have two independent IPUs (image processing units), and each IPU has two display ports. They can support up to four external ports at any given time.
- The i.MX 6DualLite and i.MX 6Solo chips have one IPU, so they can only support two display ports at a time.

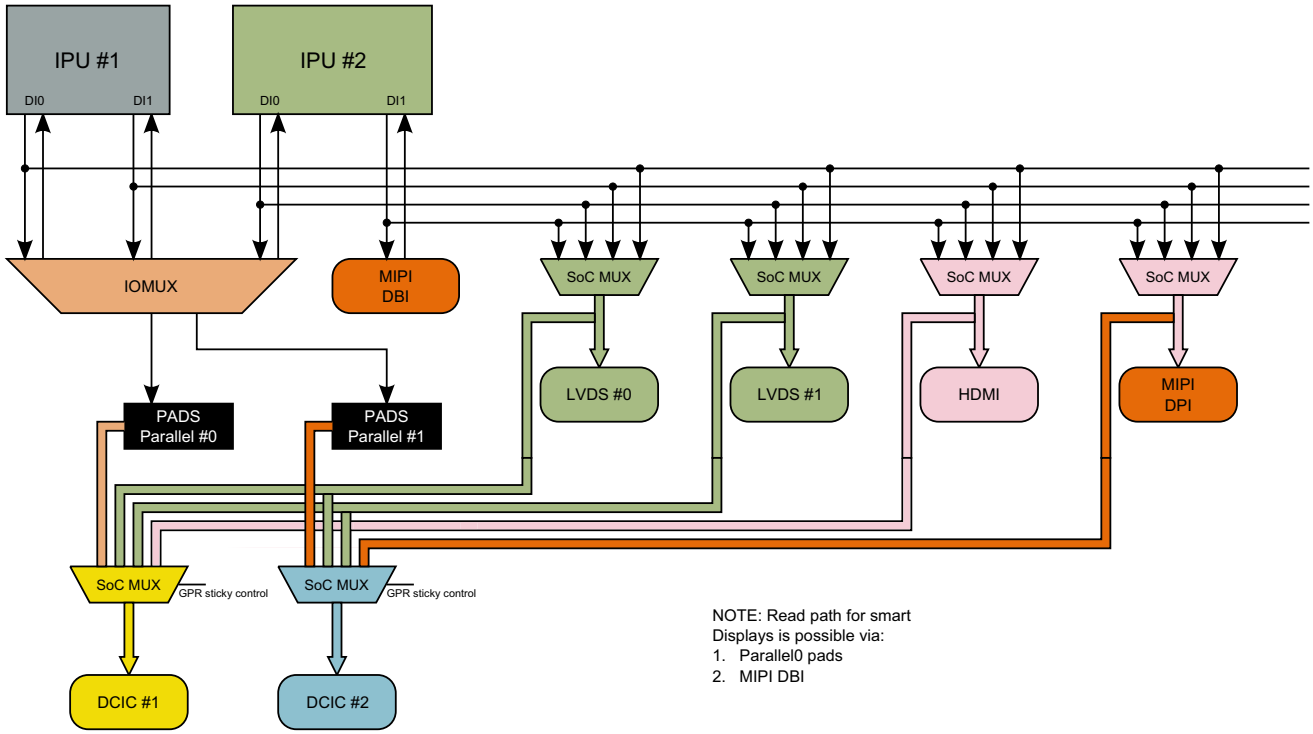


Figure 7. i.MX 6Dual/6Quad display ports muxing scheme

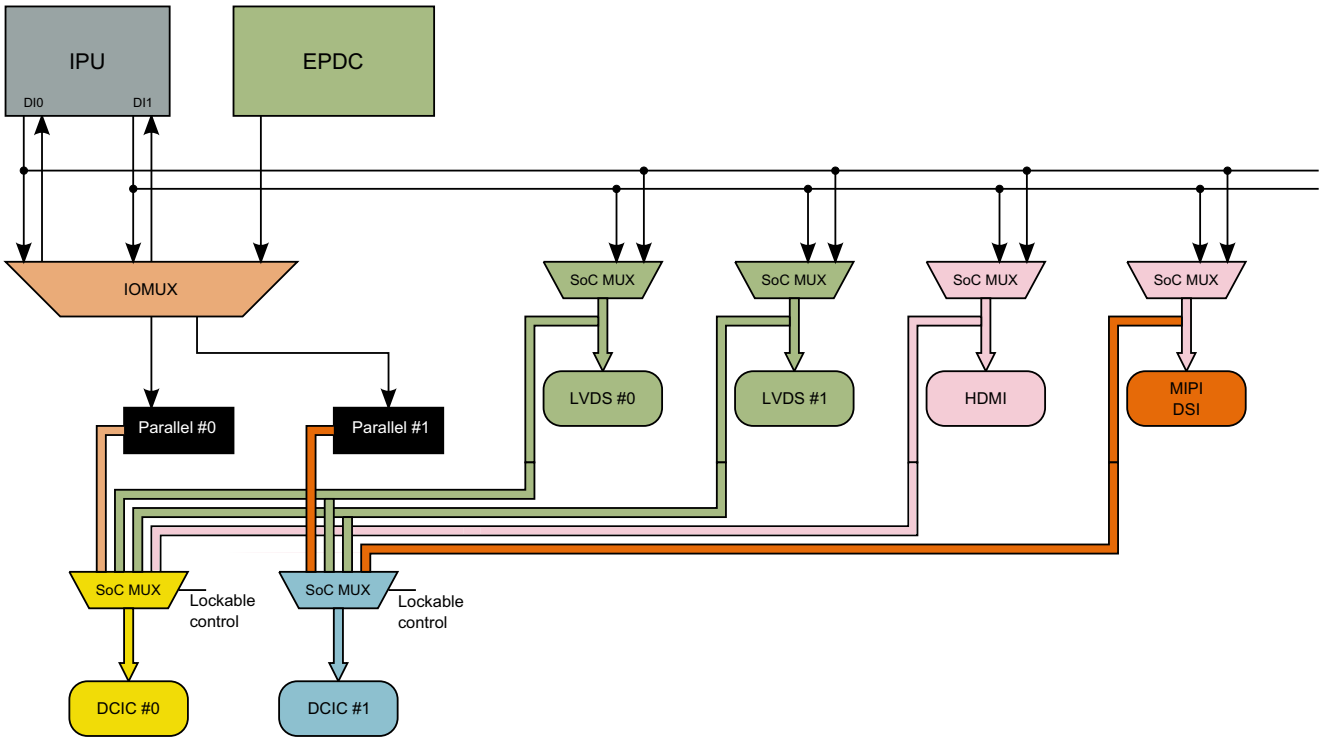


Figure 8. i.MX 6Solo/6DualLite display port muxing scheme

8 Video input requirements for migration

The figures in this section show the video input requirement differences between an i.MX 6Dual/6Quad hardware design and an i.MX 6Solo/6DualLite hardware design.

NOTE

Do not use Parallel 1 port as the video input when migrating an i.MX 6Dual/6Quad hardware design to the i.MX 6Solo/6DualLite.

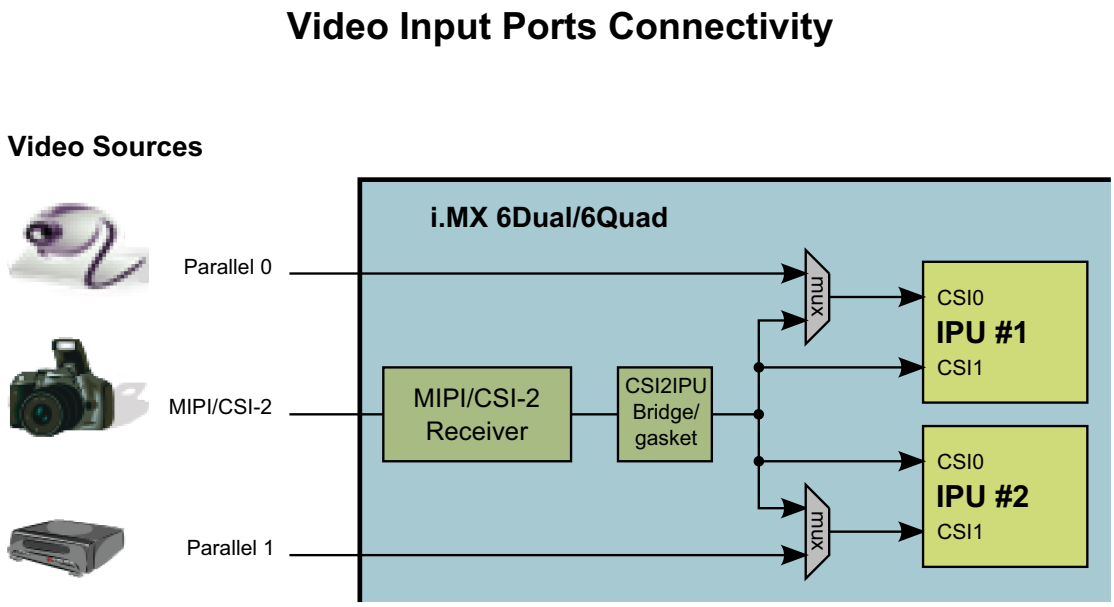


Figure 9. i.MX 6Dual/6Quad video input ports

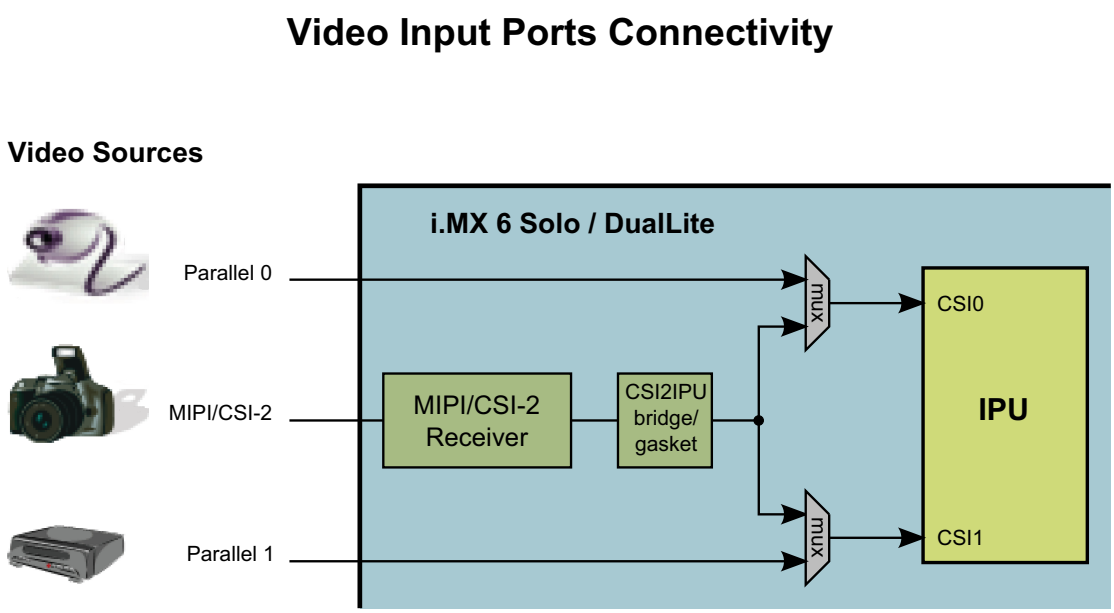


Figure 10. i.MX 6Solo/6DualLite video input ports

9 SATA requirements for migration

All SATA signals and power supplies can be left open when migrating an i.MX 6Dual/6Quad hardware design to the i.MX 6Solo/6DualLite.

10 eCSPI requirements for migration

The i.MX 6Quad, 6Dual, 6DualLite, and 6Solo chips have the following key difference in their eCSPI interfaces.

- i.MX 6Quad and i.MX 6Dual chips have five eCSPI (eCSPI1~5) interfaces. Each interface can support up to 52 Mbps.
- The i.MX 6DualLite and i.MX 6Solo chips have four eCSPI (eCSPI1~4) interfaces, and each of them can support up to 52 Mbps.

NOTE

Do not use SD1 and SD2 signals as eCSPI5 when migrating an i.MX 6Dual/6Quad hardware design to the i.MX 6Solo/6DualLite because the i.MX 6Solo/6DualLite has no eCSPI5 muxing function available on the SD1 and SD2 signals.

Table 8. eCSPI5 muxed signals in i.MX 6Dual/6Quad

Pad	Power group	ALT 1 mode	
		Instance	Port
SD2_DAT1	SD2	ecspi5	SS0
SD2_DAT2	SD2	ecspi5	SS1
SD2_DAT0	SD2	ecspi5	MISO
SD1_DAT1	SD1	ecspi5	SS0
SD1_DAT0	SD1	ecspi5	MISO
SD1_DAT3	SD1	ecspi5	SS2
SD1_CMD	SD1	ecspi5	MOSI
SD1_DAT2	SD1	ecspi5	SS1
SD1_CLK	SD1	ecspi5	SCLK
SD2_CLK	SD2	ecspi5	SCLK
SD2_CMD	SD2	ecspi5	MOSI
SD2_DAT3	SD2	ecspi5	SS3

11 I²C requirements for migration

i.MX 6DualLite and i.MX 6Solo chips have one more I²C (I2C4) than i.MX 6Quad and i.MX 6Dual chips.

Table 9. I2C4 muxing in i.MX 6Solo/6DualLite

Contact name	Mux mode ALT 8
GPIO_8	i2c4.SDA
GPIO_7	i2c4.SCL

NOTE

Reserve the GPIO_8 and GPIO_7 pins for I2C4 in i.MX 6Dual/6Quad hardware design if I2C4 will be used after migrating to i.MX 6Solo/6DualLite.

12 MIPI camera requirements for migration

The i.MX 6Dual and i.MX 6Quad chips support up to four D-PHY Rx data lanes, but the i.MX 6DualLite and i.MX 6Solo chips support two D-PHY Rx data lanes. The CSI_D2P, CSI_D2M, CSI_D3P, and CSI_D3M signals are not present in i.MX 6DualLite and i.MX 6Solo.

Use a MIPI camera with two data lanes and connect them with the CSI_D0 and CSI_D1 signals when migrating an i.MX 6Dual/6Quad hardware design to the i.MX 6Solo/6DualLite.

13 Revision history

Table 10 provides a revision history for this application note.

Table 10. Revision history

Rev. Number	Date	Substantive Change(s)
Rev. 1	5/2013	• In Figure 7, “i.MX 6Dual/6Quad display ports muxing scheme,” and Figure 9, “i.MX 6Dual/6Quad video input ports”: Changed “IPU #0” to “IPU #1,” and changed “IPU #1” to “IPU #2.” • In Figure 8, “i.MX 6Solo/6DualLite display port muxing scheme,” and Figure 10, “i.MX 6Solo/6DualLite video input ports”: Changed “IPU #0” to “IPU.”
Rev. 0	10/2012	Initial public release.

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